

**Preliminary Information****• Ultra-High Performance**

666 MByte/sec single device transfer rate
36 ns RAS access, 13.8 ns CAS access
6 ns burst cycle

• Multibank Architecture

RAS and precharge may overlap CASREAD or WRITE to different banks effectively hiding RAS/precharge time.

• Ideal Organization for Embedded Applications

Part Code	Organization	Banks	MBytes
MD904	128K x 32	16	0.5
MD905	160Kx32	20	0.562
MD906	192K x 32	24	0.75
MD908	256K x 32	32	1.0
MD909	288K x 32	36	1.125
MD910	320K x 32	40	1.25
MD916	512K x 32	64	2.0

• Fine Granularity

Quarter MByte minimum granularity.

• Variable Length Burst

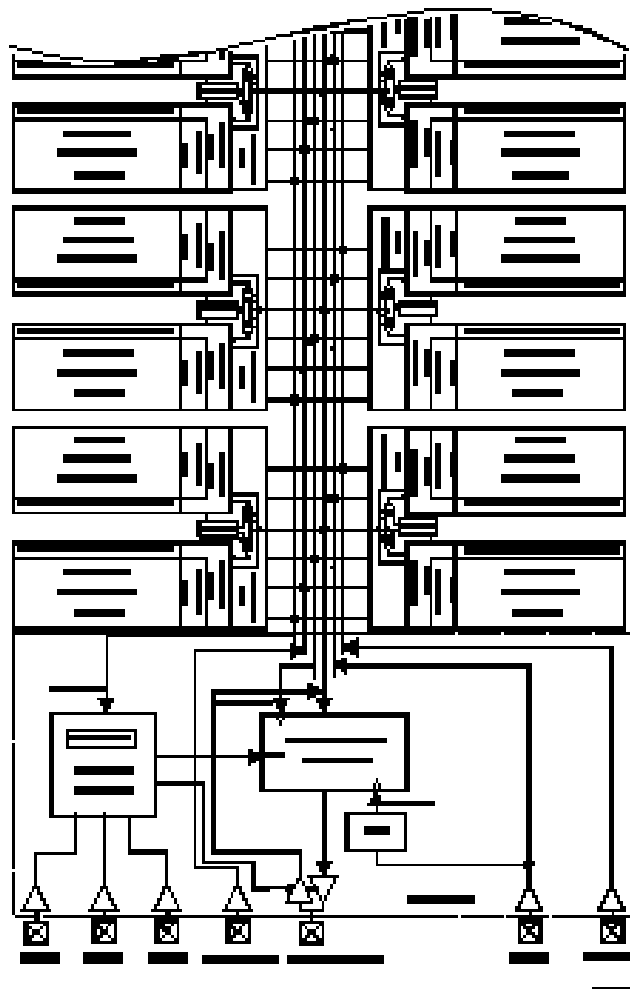
Supports 4 to 128 byte interruptable bursts

• Byte-level Write Control**• Low Internal and Interface Power.****• Small Footprint**

Up to 2.3 MByte single package: 14 mm x 20 mm
PQFP or 68 pin PLCC.

• Compact, Easily Implemented Interface

Twenty-six signal, bus interface employs
CMOS/LVCMOS/SSTL signaling.

• Both 5.0V and 3.3V Supply Option**Figure 1. MDRAM Block Diagram****Description**

The MoSys Multibank DRAM (MDRAM) is an extended performance synchronous DRAM optimized for ultra-high performance applications where high bandwidth, extremely short access latency and low cost are required. MDRAMs feature fully synchronous I/O at frequencies up to 333 MHz providing 666 MBytes per second of per device peak bandwidth.

An MDRAM can be viewed as an array of many independent 256 Kbit DRAMs, connected to a common bus internal to the MDRAM. The independence of bank facilitates overlapping, or "hiding" the RAS access and precharge penalty so that average access times will approach the CAS access time.

Embedded applications, using small amounts of DRAM (under 8 MBytes) will benefit from the MDRAM's fine gran-

ularity yielding lower cost solutions. MDRAM arrays can be created in increments of 256 KByte. An application requiring 2.75 MBytes can use precisely 2.75 MBytes of MDRAM rather than incrementing up to 4 MBytes as with any other DRAM.