

BTL driver for CD/CD-ROM

BA5995FM

The BA5995FM is 4-channel BTL driver IC for driving actuator and motor of CD-ROM. Power package of HSOP-M28 pin enables to make set smaller. This IC is available for low voltage DSP.

●Applications

CD-ROM, others

●Features

- 1) Wide dynamic range. (4V (typ.) at PreVcc=12V, PowVcc=5V, RL=8Ω)
- 2) Thermal shut down circuit built in.
- 3) Separating Vcc into Pre and Power (Power divides into CH1, 2 and CH3/4), can make better power efficiency, by low supply voltage drive.
- 4) Stand by operated individually CH2 and CH1/3/4.
- 5) Built-in mute(CH1) circuit.
- 6) Suitable for low operation voltage DSP by wide D-range pre opamp.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	PreVcc, PowVcc	13.5	V
Power dissipation	Pd	2.2 ^{*1}	W
Max output current	IO _{Max}	1 ^{*2}	A
Operating temperature range	Topr	-35 to +85	°C
Storage temperature range	Tstg	-55 to +150	°C

*1 On less than 3% (percentage occupied by copper foil), 70mm×70mm, t=1.6mm, glass epoxy mounting.
Reduce power by 17.6mW for each degree above 25°C.

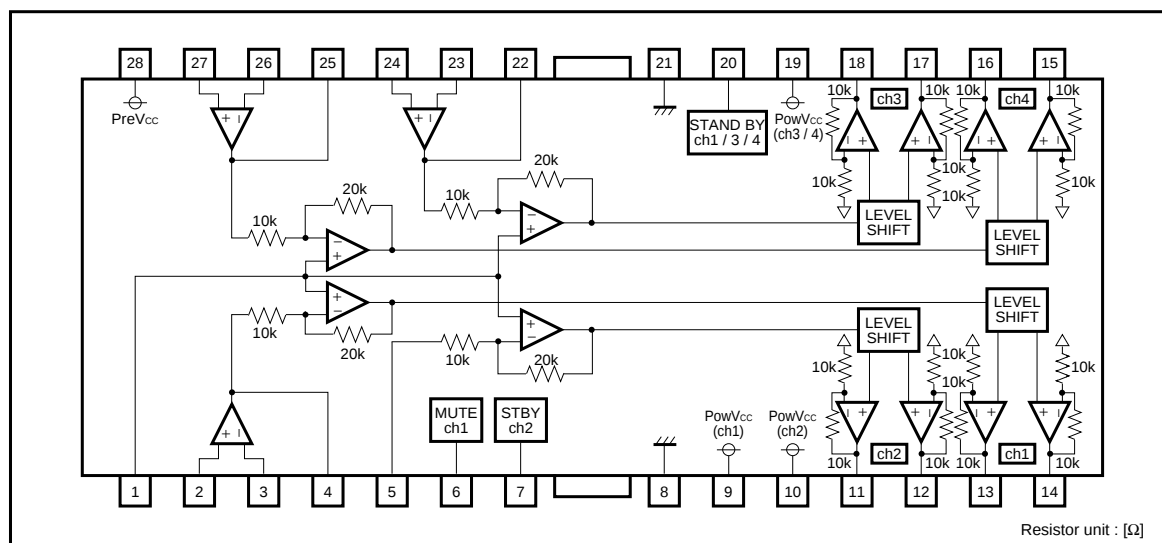
*2 The output current must not exceed the maximum Pd and ASO.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Vcc for pre block	PreVcc	4.5 to 13.2V	V
Vcc for power block	PowVcc	4.5 to PreVcc	V

Optical disc ICs

●Block diagram



●Pin descriptions

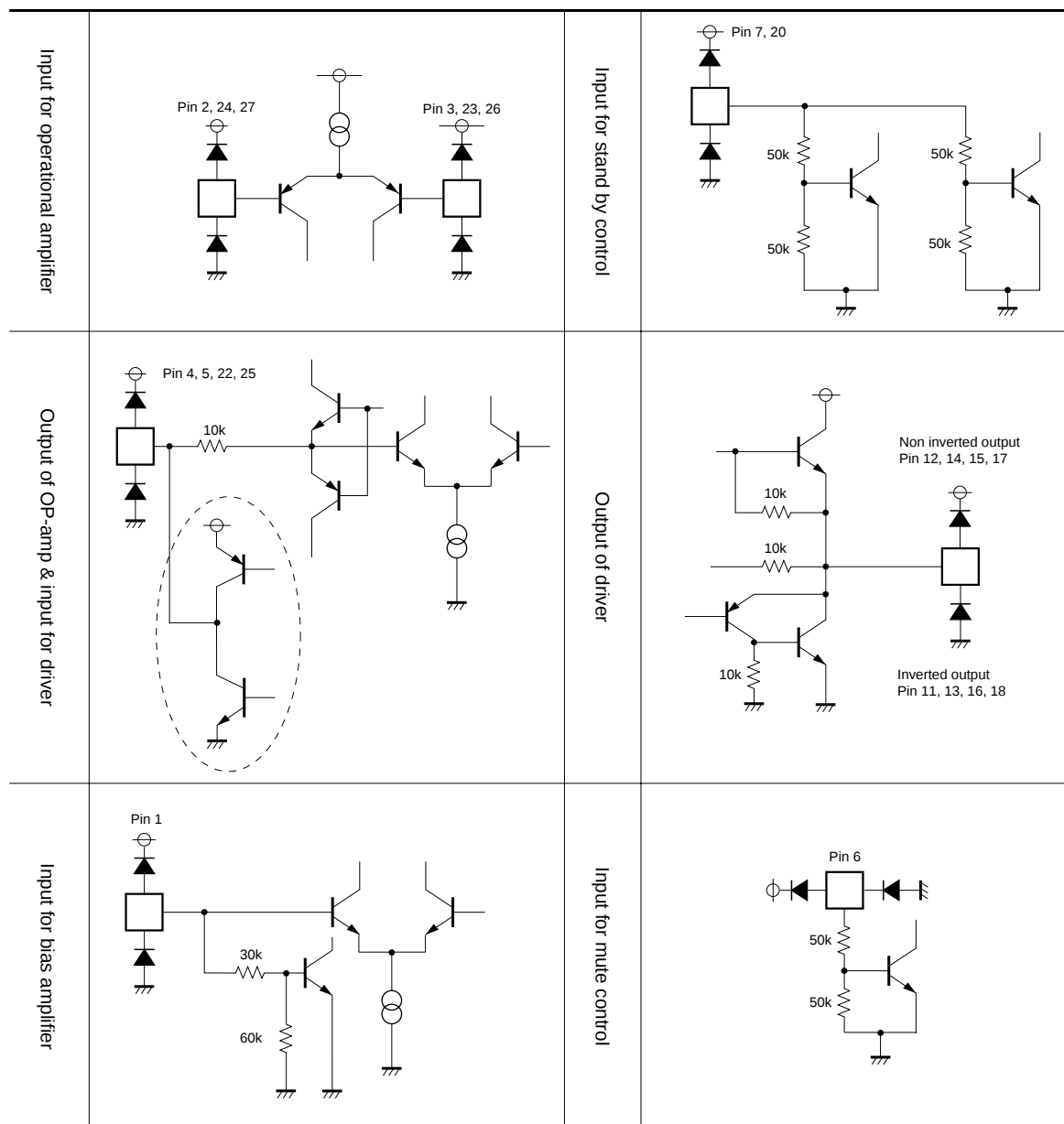
Pin No.	Pin name	Function
1	BIAS IN	Input for bias-amplifier
2	OPIN1 (+)	Non inverting input for CH1 OP-AMP
3	OPIN1 (-)	Inverting input for CH1 OP-AMP
4	OPOUT1	Output for CH1 OP-AMP
5	IN2	Input for CH2
6	MUTE	Input for CH1 mute control
7	STBY2	Input for CH2 stand by control
8	GND	Substrate ground
9	PowVcc1	Vcc for CH1 power block
10	PowVcc2	Vcc for CH2 power block
11	Vo2 (-)	Inverted output of CH2
12	Vo2 (+)	Non inverted output of CH2
13	Vo1 (-)	Inverted output of CH1
14	Vo1 (+)	Non inverted output of CH1

Note) Symbol of + and - (output of drivers) means polarity to input pin.
(For example if voltage of pin4 high, pin14 is high.)

Pin No.	Pin name	Function
15	Vo4 (+)	Non inverted output of CH4
16	Vo4 (-)	Inverted output of CH4
17	Vo3 (+)	Non inverted output of CH3
18	Vo3 (-)	Inverted output of CH3
19	PowVcc3	Vcc for CH3/4 power block
20	STBY1	Input for CH1/3/4 stand by control
21	GND	Substrate ground
22	OPOUT3	Output for CH3 OP-AMP
23	OPIN3 (-)	Inverting input for CH3 OP-AMP
24	OPIN3 (+)	Non inverting input for CH3 OP-AMP
25	OPOUT4	Output for CH4 OP-AMP
26	OPIN4 (-)	Inverting input for CH4 OP-AMP
27	OPIN4 (+)	Non inverting input for CH4 OP-AMP
28	PreVcc	Vcc for pre block

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●Input output circuits

Resistor unit : [Ω]

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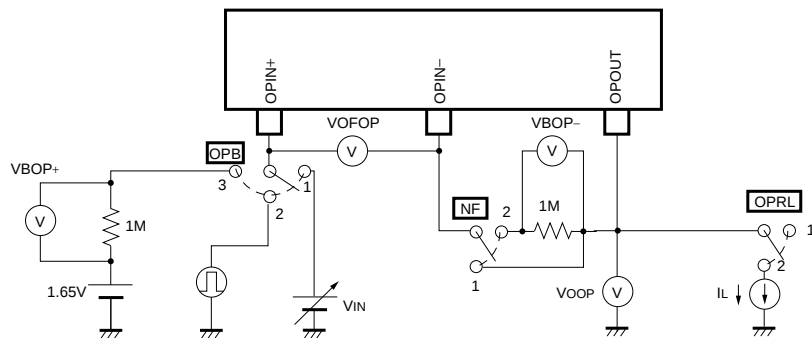
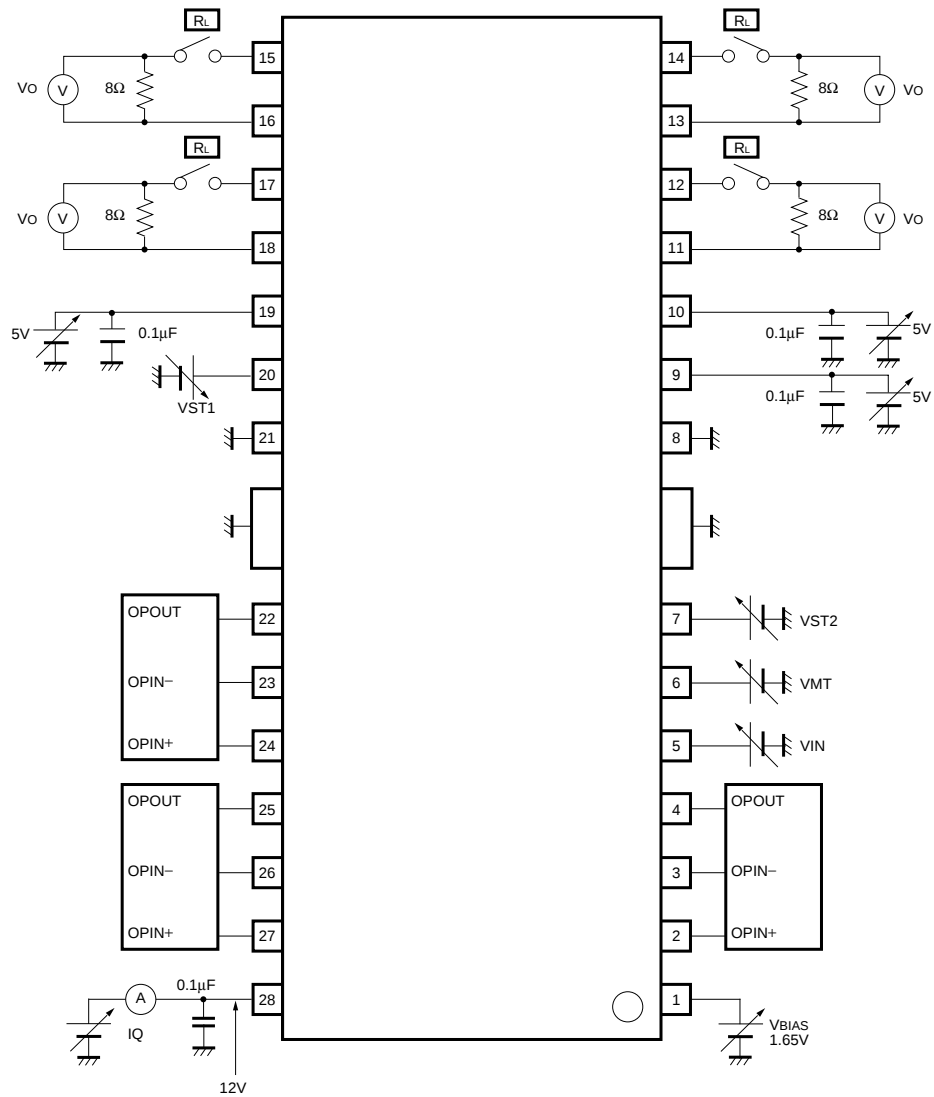
●**Electrical characteristics** (unless otherwise noted, Ta=25°C, PreV_{CC}=12V, PowV_{CC}=5V, V_{BIAS}=1.65V, R_L=8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I _Q	–	20	30	mA	R _L = ∞
CH1/3/4 standby current	I _{QST1}	–	5.2	12	mA	R _L = ∞
CH2 standby current	I _{QST2}	–	16	26	mA	R _L = ∞
All channel standby current	I _{QST3}	–	–	1	mA	R _L = ∞
<Driver block>						
Output offset voltage 1	V _{OOF}	–70	0	70	mV	
Maximum output voltage 1	V _{OM1}	3.6	4.0	–	V	V _{IN} =V _{BIAS} ±1.65V
Maximum output voltage 2	V _{OM2}	7.5	9.0	–	V	V _{IN} =V _{BIAS} ±1.65V PowV _{CC} =12V
Closed loop voltage gain	G _{VC}	16.6	17.6	18.6	dB	V _{IN} =V _{BIAS} ±0.3V
Slew rate	S _{RDRV}	–	2	–	V/μs	Input pulse 100kHz, 2V _{P-P}
Standby on voltage	V _{STON}	–	–	0.5	V	
Standby off voltage	V _{STOFF}	2.0	–	–	V	
Bias drop mute on voltage	V _{BMON}	–	–	0.7	V	
Bias drop mute off voltage	V _{BMOFF}	1.3	–	–	V	
Mute on voltage	V _{MTON}	2.0	–	–	V	
Mute off voltage	V _{MTOFF}	–	–	0.5	V	
Output voltage on muting	V _{MO}	–0.5	0	0.5	mV	t _m =125μsec
<Pre operational amplifier>						
Common mode input range	V _{OFOF}	0	–	9.0	V	
Input offset voltage	I _{BOP}	–6	0	6	mV	
Input bias current	V _{OHOP}	–	–	300	nA	I _L =+300μA, V _{IN} =3.3V
High level output voltage	V _{OLOP}	–6	0	6	mV	I _L =–1mA
Low level output voltage	S _{ROP}	–	0.1	0.3	V	Input pulse 100kHz, 2V _{P-P}
Slew rate		–	2	–	V/μs	

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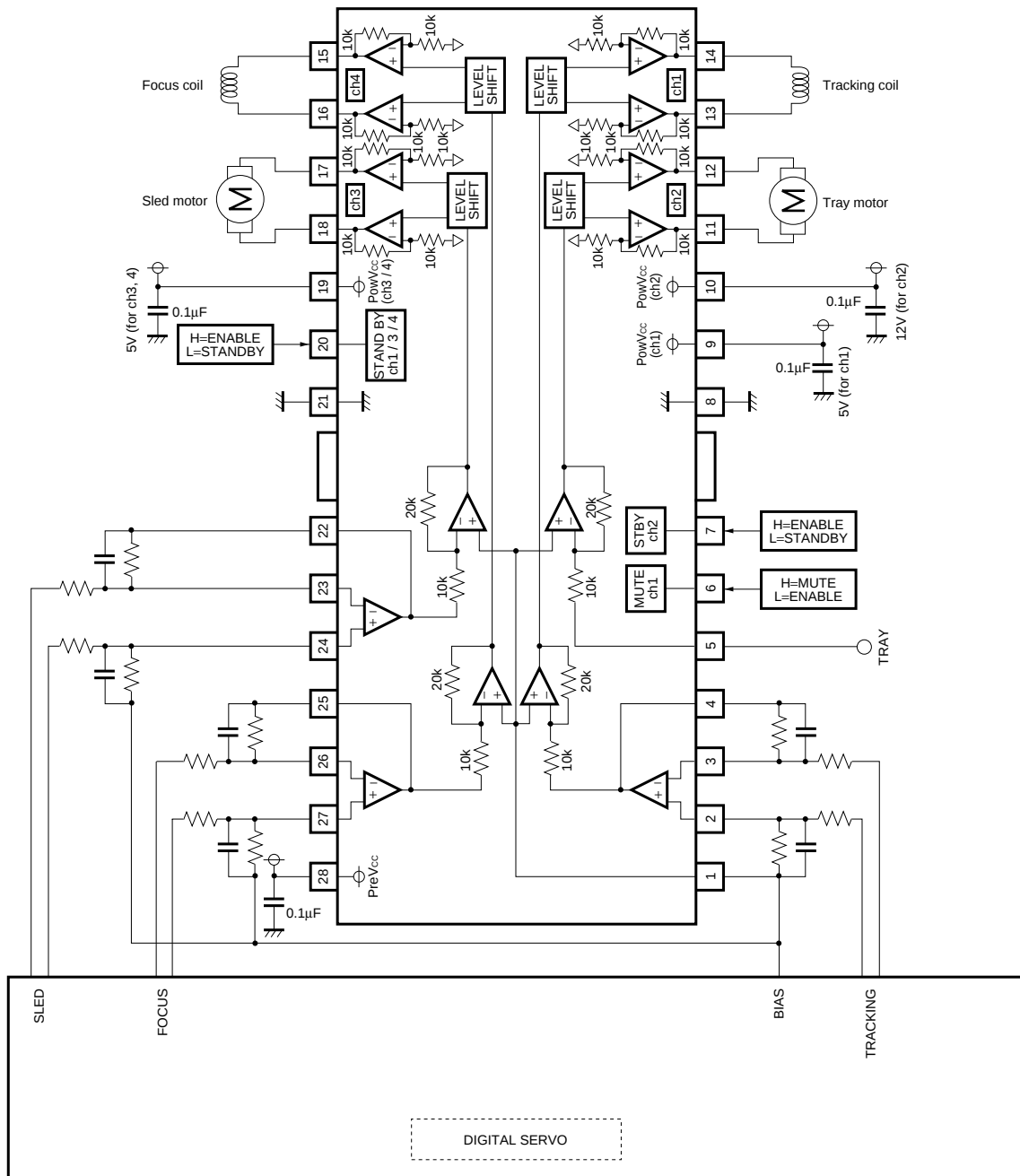
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●Measurement circuit

Resistor unit : [Ω]

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●Application example



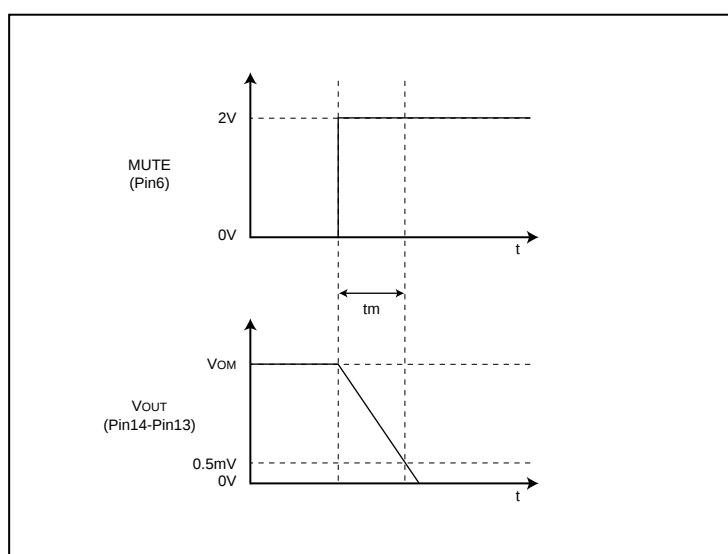
Resistor unit : [Ω]

Fig.2

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●Operation notes

- (1) Thermal shut down circuit is built in. In case IC chip temperature rises to 175°C(typ.), thermal shut down circuit operates and muted the output current. Next time IC chip temperature falls below 150°C(typ.), the driver blocks start.
- (2) Bias pin (pin1) should be pulled up more than 1.3V. In case bias pin voltage is under 0.7V(typ.), output current is muted.
- (3) In case supply voltage falls below 3.8V(typ.), output current is muted. Next time supply voltage rises to 4.0V (typ.), the driver blocks start.
- (4) Mute operation is caused by thermal shut down, decrease of bias pin voltage or decrease of supply voltage.
When mute is done, output voltage becomes internal reference voltage (about $PowV_{CC}/2$).
- (5) In case of one of the standby terminals turn into or open , correspondence channel circuit (include opamps) is muted.
- (6) Both of the standby terminals low or open, all circuits shutdown (sleep mode) and all output pins become high impedance. In addition to threshold is 1.4V(typ.).
- (7) Supply voltage of $PreV_{CC}$ should be equal to or higher than $PowV_{CC}$.
- (8) Take care the external resistor value of OPamp .
OPamp source current supplies to internal resistor (10K Ω) as well as external resistor.
- (9) Insert the by pass capacitor between V_{CC} pin and GND pin of IC as near as possible (approximately 0.1 μ F).
- (10) Keep the GND pin voltage the lowest of all pins .
- (11) Heat dissipation fins are attached to the GND on the inside of the package. Make sure to connect these to the external GND.
- (12) If the mute pin (pin6) voltage rises above 2.0V, the output (CH1) current can be muted.
Under normal operating conditions, make sure to open pin7 or pull it down below 0.5V.
Next figure is high impedance mute timing chart.



$PreV_{CC}=12V$
 $PowV_{CC1}=5V$
 $BIAS=1.65V$
 $R_L=8\Omega$
 $t_m \leq 125\mu sec$

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●Electrical characteristic curves

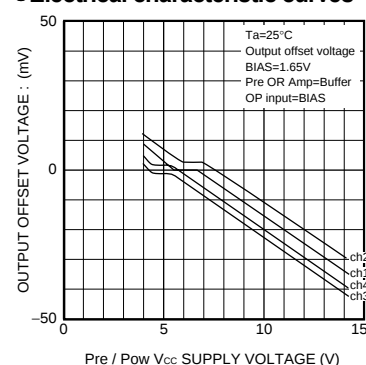


Fig.3 Output offset voltage vs. power supply voltage characteristic

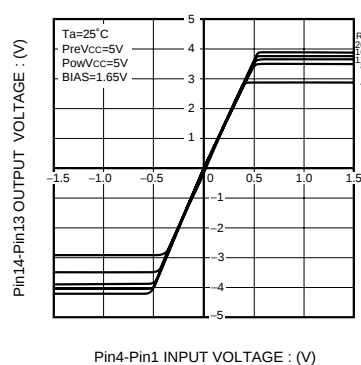


Fig.4 I/O characteristic (ch1)

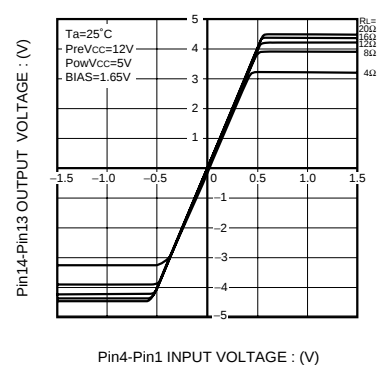


Fig.5 I/O characteristic (ch1)

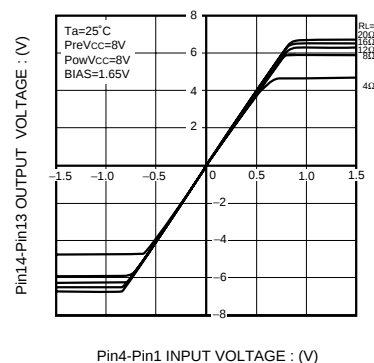


Fig.6 I/O characteristic (ch1)

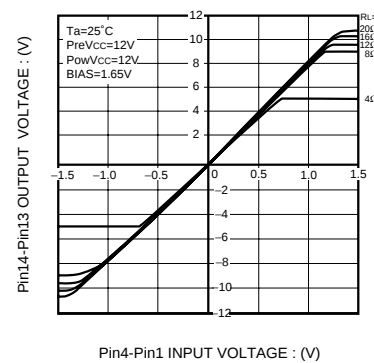


Fig.7 I/O characteristic (ch1)

●External dimensions (Units : mm)

