

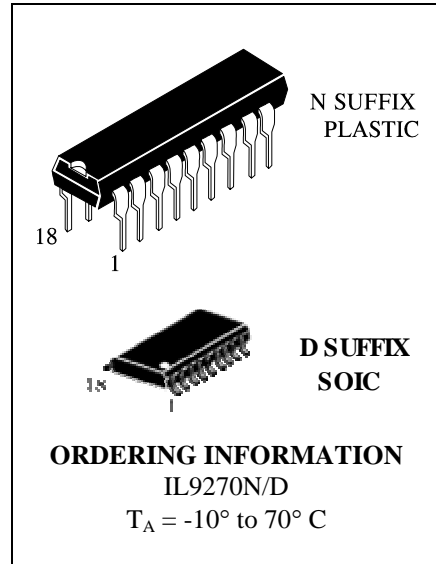
DTMF RECEIVER

High-Performance Silicon-Gate CMOS

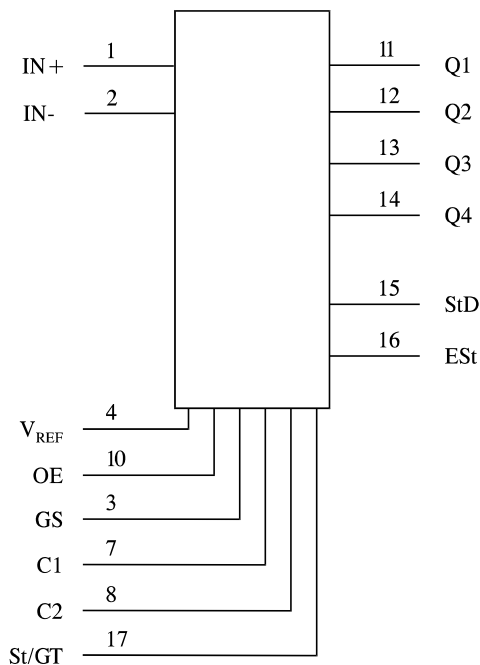
IL9270

The IL9270N/D is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high- and low-group filters and dial-tone rejection. Digital counting techniques are employed in the decoder to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on-chip provision of a differential input amplifier, clock-oscillator and latched 3-state bus interface.

- Complete receiver in an 18-pin package.
- Excellent performance.
- CMOS, single 5 volt operation.
- Minimum board area.
- Central office quality.
- Low power consumption.

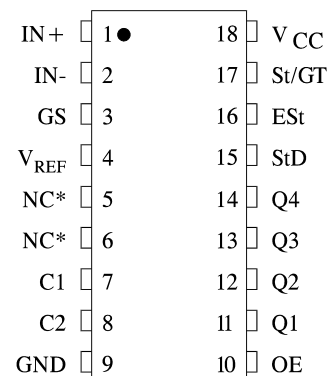


LOGIC DIAGRAM



PIN 9 = GND
PIN 18 = V_{CC}
PINS 5,6 = NO CONNECTION

PIN ASSIGNMENT



* Connect to GND

PIN DESCRIPTIONS

| NAME | PIN | DESCRIPTION | |
|-----------|-------|---|--|
| ESt | 16 | Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low. | |
| GS | 3 | Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor. | |
| IC | 5,6 | Internal Connection. Must be tied to GND. | |
| IN+ | 1 | Non-Inverting Input | Connections to the front-end differential amplifier. |
| IN- | 2 | Inverting Input | |
| C1 | 7 | Clock Input | 3.579545 MHz crystal connected between these pins completes internal oscillator. |
| C2 | 8 | Clock Output | |
| Q1-Q4 | 11-14 | 3-state data outputs. When enabled by OE, provide the code corresponding to the last valid tone-pair received. | |
| StD | 15 | Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt} . | |
| St/GT | 17 | Steering input/guard time output (bi-directional). A voltage greater than V_{TSt} , detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St. | |
| OE | 10 | 3-state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull-up. | |
| V_{CC} | 18 | Positive power supply, +5 V. | |
| V_{REF} | 4 | Reference voltage output, nominally $V_{CC} / 2$. May be used to bias the inputs at mid-rail. | |
| GND | 9 | Negative power supply, normally connected to 0 V. | |

FUNCTIONAL DESCRIPTION

The IL9270 monolithic DTMF receivers offer small size, low power consumption and high performance. The architecture consists of a bandsplit filter section, which separates the high and low tones of a receiver pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two filters - a sixth order for the high group and an eight

order for the low group. The band-widths of which correspond to the bands enclosing the low-group and high-group tones (see Figure 1). The filter section also incorporates notches at 350 Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a second order switched-capacitor section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The decoder uses digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to “talk-off” and tolerance to the presence of interfering signals (“third tones”) and noise. When the detector recognizes the simultaneous presence of two valid tones (referred to as “signal condition” in some industry specifications), it raises the “early steering” flag (ESt). Any subsequent loss of signal-condition will cause Est to fall.

Steering Circuit

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as “character-recognition-condition”). This check is performed by an external RC time-constant driven by ESt. A logic high on ESt causes V_C (see Figure 2) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone-pair, latching its corresponding 4-bit code (see Figure 3) into the output latch. At this point, the GT output is activated and drives V_C to V_{CC} . GT continues to drive high as long as ESt remains high. Finally after a short delay to allow the output latch to settle, the “delayed-steering” output flag, StD, goes high, signaling that a received tone-pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the 3-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (“drop-out”) too short to be considered a valid pause. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Figure 2 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μ F is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 ms would be 300 k.

Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and inter-digital pause.

Guard-time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard-time adjustment is shown in Figure 4.

Input Configuration

The input arrangement of the IN9270 provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 5 with the op-amp connected for unity gain and V_{REF} biasing the input at $1/2V_{CC}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5 .

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|----------|---|------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.3 to +6.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.3 to $V_{CC} + 0.3$ | V |
| I_{IN} | DC Input Current, per Pin | 10 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP** | 500 | mW |
| Tstg | Storage Temperature | -65 to +150 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

** Derating: $-10 \text{ mW}/^{\circ}\text{C}$ from 65°C to 70°C .

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------|--|------|------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.75 | 5.25 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | 1.5 | 3.5 | V |
| T_A | Operating Temperature | -10 | +70 | °C |
| P_O | Power Consumption ($f = 3.579 \text{ MHz}$, $V_{CC} = 5 \text{ V}$) | - | 45 | mW |
| t_r , t_f | Input Rise and Fall Time | 0 | 110 | ns |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $\text{GND} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND, $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = -10\text{ to }+70^\circ\text{C}$)

| Symbol | Parameter | Test Conditions | Guaranteed Limits | | | Unit |
|-----------|--|--|-------------------|-----|-----------|------------------|
| | | | Min | Typ | Max | |
| V_{IH} | Minimum High-Level Input Voltage | $V_{OUT} = 5\text{ V}$ | 3.6 | | | V |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{OUT} = 5\text{ V}$ | | | 1.4 | V |
| V_{OH} | Minimum High-Level Output Voltage | No Load | 4.97 | | | V |
| V_{OL} | Maximum Low-Level Output Voltage | No Load | | | 0.05 | V |
| I_{IN} | Maximum Input Leakage Current | $V_{IN} = V_{CC}$ or GND | | | ± 0.1 | μA |
| I_{SO} | Maximum Pull Up (Source) Current | $OE = 0\text{ V}$ | | | 24 | μA |
| I_{OL} | Minimum Output-Low (Sink) Current | $V_{OUT} = 0.4\text{ V}$ | 0.8 | | | mA |
| I_{OH} | Minimum Output-High (Source) Current | $V_{OUT} = 4.6\text{ V}$ | 0.35 | | | mA |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | $V_{IN} = V_{CC}$ | | | 11 | mA |
| V_{TSt} | Steering Threshold Voltage | | 2.2 | | 2.5 | V |
| R_{IN} | Input Impedance (Signal Inputs 1,2) | @ 1 KHz | 8 | | | $\text{M}\Omega$ |
| V_{REF} | Output Voltage | No Load | 2.4 | | 2.8 | V |
| R_{OR} | Output Resistance | | | 10 | | $\text{k}\Omega$ |
| I_{OZ} | Maximum Three-State Leakage current | Output in High-Impedance State $V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$ or GND | | | ± 0.1 | μA |

OPERATING CHARACTERISTICS

Gain Setting Amplifier

| Symbol | Parameter | Test Conditions | Typ | Unit |
|-----------|--------------------------------|---|-----------|-----------------|
| I_N | Input Leakage Current | $GND < V_{IN} < V_{CC}$ | ± 100 | nA |
| R_{IN} | Input Resistance | | 10 | M Ω |
| V_{OS} | Input Offset Voltage | | ± 25 | mV |
| PSRR | Power Supply Rejection | 1 KHz | 60 | dB |
| CMRR | Common Mode Rejection | $-3.0 \text{ V} < V_{IN} < 3.0 \text{ V}$ | 60 | dB |
| A_{VOL} | DC Open Loop Voltage Gain | | 65 | dB |
| f_c | Open Loop Unity Gain Bandwidth | | 1.5 | MHz |
| V_O | Output Voltage Swing | $R_L \geq 100 \text{ K}\Omega$ to GND | 4.5 | V _{PP} |
| C_L | Tolerable Resistive Load (GS) | | 100 | pF |
| $R_{L:}$ | Tolerable Resistive Load (GS) | | 50 | K Ω |
| V_{CM} | Common Mode Range | No Load | 3.0 | V _{PP} |

AC ELECTRICAL CHARACTERISTICS (All Voltages referenced to GND. $V_{CC} = 5.0 \text{ V}$, $GND = 0 \text{ V}$, $T_A = -10$ to $+70^\circ\text{C}$, $F_{CLK} = 3.579545 \text{ Mhz}$, using test circuit of Figure 5)

| Parameter | | Guaranteed Limits | | | Unit | Notes |
|--|-----|-------------------|------|-----------------------------------|--------------------|----------------|
| | | Min | Typ | Max | | |
| SIGNAL CONDITION | | | | | | |
| Valid Input Signal Level (each tone of composite signal) | MIN | | | -29 | dBm | 1,2,3,5,6,9 |
| | | | | 27.5 | m V _{RMS} | 1,2,3,5,6,9 |
| | MAX | +1 | | | dBm | 1,2,3,5,6,9 |
| | | 883 | | | m V _{RMS} | |
| NON-ACCEPT LEVEL | | | | | | |
| Freq. Deviation Accept Limit | | | | $\pm 1.5\%$ $\pm 2 \text{ Hz}$ | Nom. | 2,3,5,9 |
| Freq. Deviation Reject Limit | | $\pm 3.5\%$ | | | Nom. | 2,3,5 |
| Third Tone Tolerance | | | -2.5 | | dB | 2,3,4,5,7,9,10 |
| Dial Tone Tolerance | | | +18 | | dB | 2,3,4,5,8,9,10 |

TIMING REQUIREMENTS (All Voltages referenced to GND. $V_{CC} = 5.0\text{ V}$, $GND = 0\text{ V}$, $T_A = -10\text{ to }+70^\circ\text{C}$, $F_{CLK} = 3.579545\text{ Mhz}$, using test circuit of Figure 5)

| Symbol | Parameter | | Guaranteed Limits | | Unit | Notes |
|----------------------|--|-----------------|-------------------|-------|---------------|----------------------------------|
| | | | Min | Max | | |
| t_{DP} | Tone Present Detection Time (Figure 7) | | 5 | 18 | ms | Refer to Fig. 7 |
| t_{DA} | Tone Absent Detection Time (Figure 7) | | 0.5 | 10 | ms | |
| t_{REC} | Maximum Tone Detection Accept (Figure 7) | | | 40 | ms | (User Adjustable) |
| \overline{t}_{REC} | Minimum Tone Detection Reject (Figure 7) | | 20 | | ms | Refer to "Guard Time Adjustment" |
| t_{ID} | Maximum Interdigit Pause Accept (Figure 7) | | | 40 | ms | |
| t_{DO} | Minimum Interdigit Pause Reject (Figure 7) | | 20 | | ms | |
| t_{PQ} | Maximum Propagation Delay (St to Q) (Figure 7) | | | 11 | μs | OE = V_{CC} |
| t_{PSED} | Maximum Propagation Delay (St to StD) (Figure 7) | | | 16 | μs | |
| t_{QSED} | Maximum Output Data Set Up (Q to StD) (Figure 7) | | | 5 | μs | |
| t_{PTE} | Maximum Propagation Delay | ENABLE | | 75 | ns | |
| t_{PTD} | (OE to Q) (Figure 7) | DISABLE | | 460 | ns | |
| f_{CLK} | Crystal/Clock Frequency | | 3.5759 | 3.581 | MHz | |
| C_{LO} | Clock Output (C2) | Capacitive Load | | 30 | pF | |

- Notes:**
1. dBm = decibels above or below a reference power of 1 mW into a 600 Ω load.
 2. Digit sequence consists of all 16 DTMF tones.
 3. Tone duration = 40 ms, Tone pause = 40 ms.
 4. Nominal DTMF frequencies are used.
 5. Both tones in the composite signal have an equal amplitude.
 6. Tone pair is deviated by $\pm 1.5\% \pm 2\text{ Hz}$.
 7. Bandwidth limited (3 KHz) Gaussian Noise.
 8. The precise dial tone frequencies are (350 Hz and 440 Hz) $\pm 2\%$.
 9. For an error rate of less than 1 in 10,000.
 10. Referenced to the lowest level frequency component in DTMF signal.

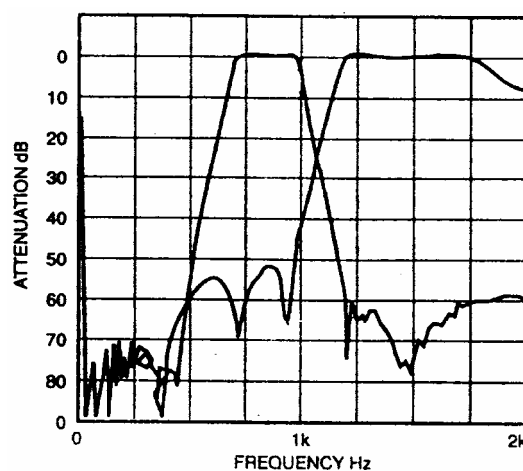


Figure 1. Typical Filter Characteristic

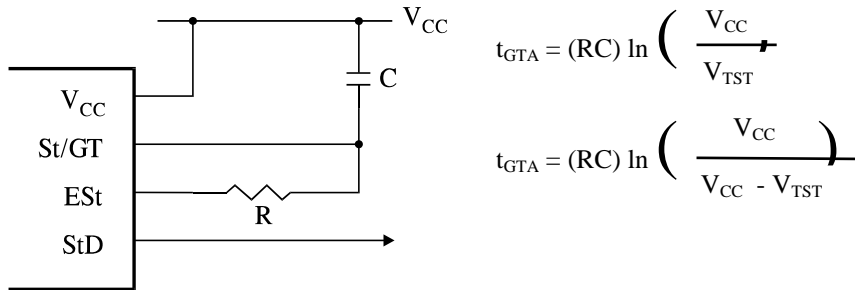


Figure 2. Basic Steering Circuit

| F _{LOW} | F _{HIGH} | KEY | OE | Q4 | Q3 | Q2 | Q1 |
|------------------|-------------------|-----|----|----|----|----|----|
| 697 | 1209 | 1 | H | 0 | 0 | 0 | 1 |
| 697 | 1336 | 2 | H | 0 | 0 | 1 | 0 |
| 697 | 1477 | 3 | H | 0 | 0 | 1 | 1 |
| 770 | 1209 | 4 | H | 0 | 1 | 0 | 0 |
| 770 | 1336 | 5 | H | 0 | 1 | 0 | 1 |
| 770 | 1477 | 6 | H | 0 | 1 | 1 | 0 |
| 852 | 1209 | 7 | H | 0 | 1 | 1 | 1 |
| 852 | 1336 | 8 | H | 1 | 0 | 0 | 0 |
| 852 | 1477 | 9 | H | 1 | 0 | 0 | 1 |
| 941 | 1336 | 0 | H | 1 | 0 | 1 | 0 |
| 941 | 1209 | * | H | 1 | 0 | 1 | 1 |
| 941 | 1477 | # | H | 1 | 1 | 0 | 0 |
| 697 | 1633 | A | H | 1 | 1 | 0 | 1 |
| 770 | 1633 | B | H | 1 | 1 | 1 | 0 |
| 852 | 1633 | C | H | 1 | 1 | 1 | 1 |
| 941 | 1633 | D | H | 0 | 0 | 0 | 0 |
| | | ANY | L | Z | Z | Z | Z |

“L = Logic Low, H = Logic High, Z = High Impedance”

Figure 3. Logic Table

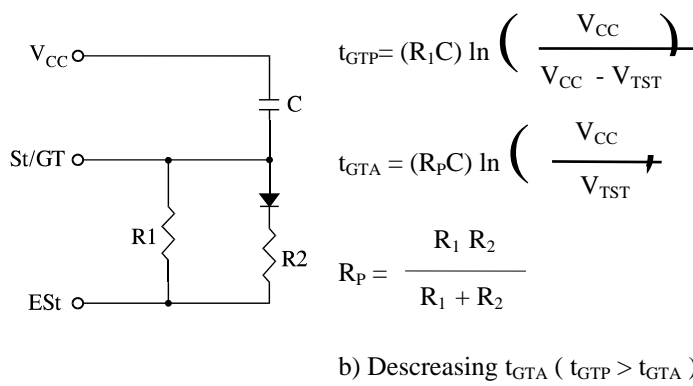
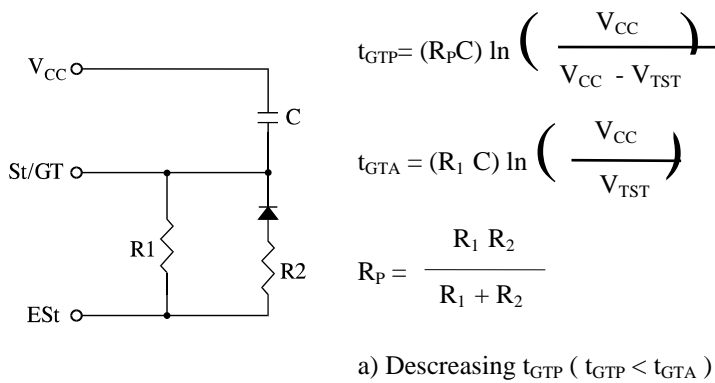


Figure 4. Guard Time Adjustment

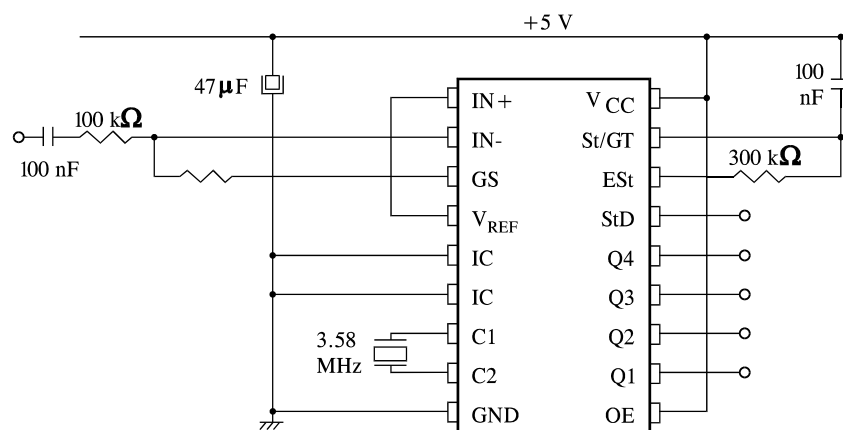


Figure 5. Single Ended Input Configuration

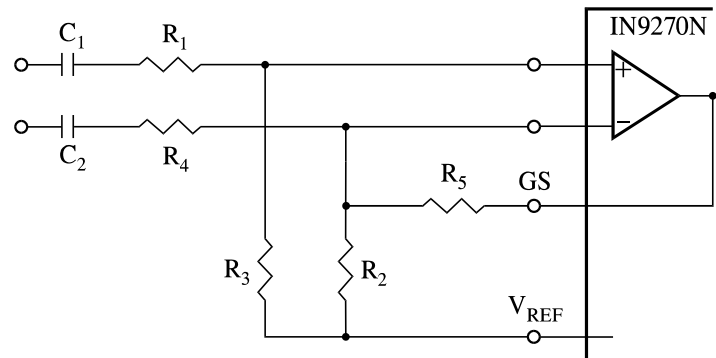
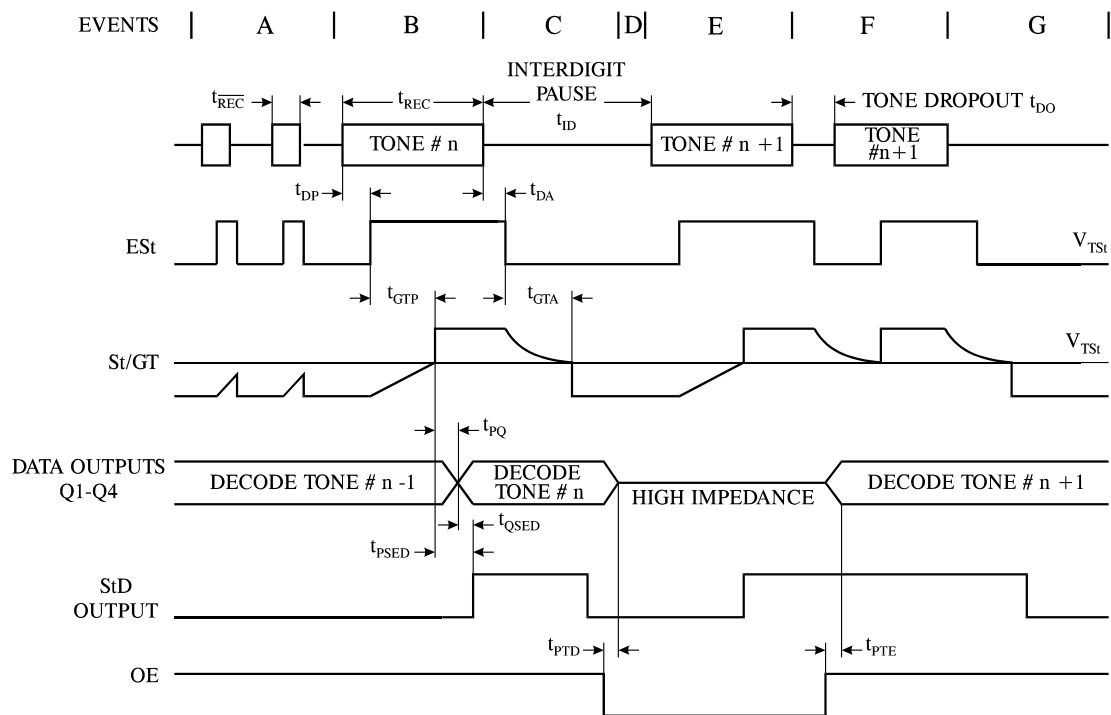


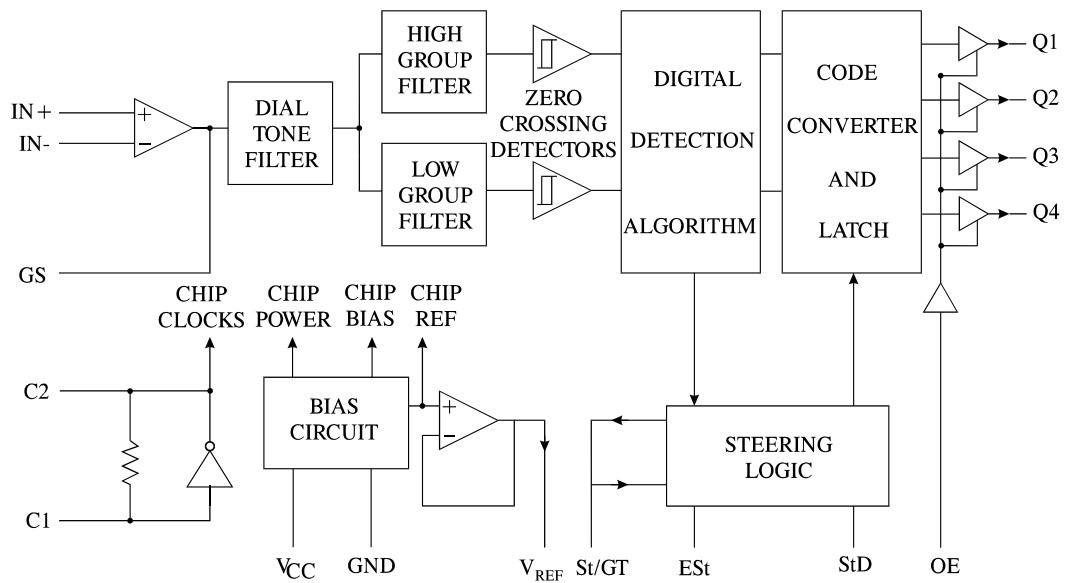
Figure 6. Differential Input Configuration

TIMING DIAGRAM

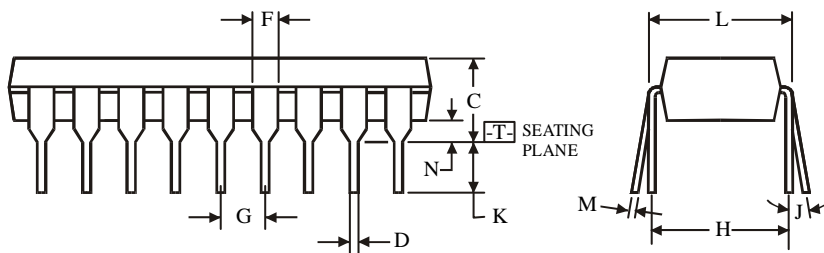
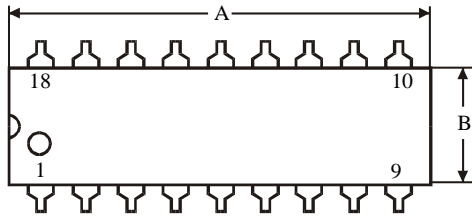
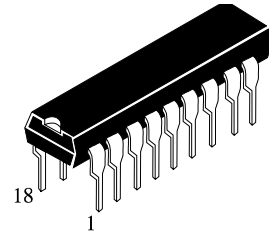


- A. Short tone bursts: detected. Tone duration is invalid.
- B. Tone #n is detected. Tone duration is valid. Decoded to outputs.
- C. End of tone #n is detected and validated.
- D. 3 State outputs disabled (high impedance).
- E. Tone #n+1 detected. Tone duration is valid. Decoded to outputs.
- F. Tristate outputs are enabled. Acceptable drop out of tone #n+1 does not register at outputs.
- G. End of tone #n+1 is detected and validated.

EXPANDED LOGIC DIAGRAM



**N SUFFIX PLASTIC DIP
(MS - 001AC)**



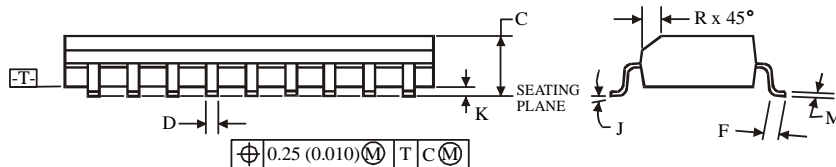
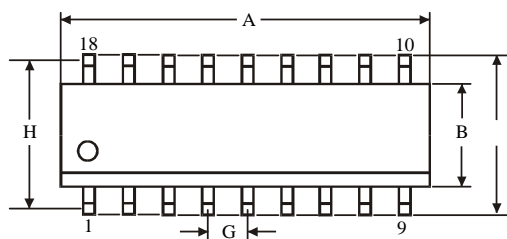
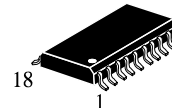
$\oplus 0.25 (0.010) \text{M} \text{T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|-------|
| | MIN | MAX |
| A | 22.35 | 23.37 |
| B | 6.1 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.2 | 0.36 |
| N | 0.38 | |

**D SUFFIX SOIC
(MS - 013AD)**



$\oplus 0.25 (0.010) \text{M} \text{T} \text{C} \text{M}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|-------|
| | MIN | MAX |
| A | 10.1 | 10.5 |
| B | 7.4 | 7.6 |
| C | 2.35 | 2.65 |
| D | 0.33 | 0.51 |
| F | 0.4 | 1.27 |
| G | 1.27 | |
| H | | |
| J | 0° | 8° |
| K | 0.1 | 0.3 |
| M | 0.23 | 0.32 |
| P | 10 | 10.65 |
| R | 0.25 | 0.75 |