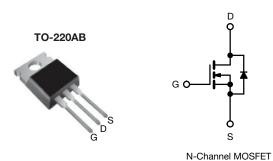
HALOGEN FREE



## **Power MOSFET**



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	100			
$R_{DS(on)}(\Omega)$	$V_{GS} = 10 \text{ V}$	0.077		
Q <sub>g</sub> max. (nC)	72			
Q <sub>gs</sub> (nC)	11			
Q <sub>gd</sub> (nC)	32			
Configuration	Single			

#### **FEATURES**

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- 175 °C operating temperature
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

#### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

# DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF540PbF
Lead (Pb)-free and halogen-free	IRF540PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub>	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			$V_{DS}$	100	V	
Gate-source voltage			$V_{GS}$	± 20	V	
Continuous drain current	V -140.V	$T_{\rm C} = 25  ^{\circ}{\rm C}$ $T_{\rm C} = 100  ^{\circ}{\rm C}$	- I <sub>D</sub>	28		
	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C		20	Α	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	110		
Linear derating factor				1.0	W/°C	
Single pulse avalanche energy <sup>b</sup>			E <sub>AS</sub>	230	mJ	
Repetitive avalanche current a			I <sub>AR</sub>	28	А	
Repetitive avalanche energy <sup>a</sup>			E <sub>AR</sub>	15	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		$P_{D}$	150	W	
Peak diode recovery dV/dt <sup>c</sup>			dV/dt	5.5	V/ns	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For	10 s		300		
Mounting torque	6.00.0*1	0.00 - 140		10	lbf ⋅ in	
	6-32 or M3 screw			1.1	N⋅m	

#### **Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b.  $V_{DD}$  = 25 V, starting  $T_J$  = 25 °C, L = 440  $\mu$ H,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 28 A (see fig. 12)
- c.  $I_{SD} \le 28 \text{ A}$ ,  $dI/dt \le 170 \text{ A/}\mu\text{s}$ ,  $V_{DD} \le V_{DS}$ ,  $T_J \le 175 \text{ °C}$
- d. 1.6 mm from case



# Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62		
Case-to-sink, flat, greased surface	R <sub>thCS</sub>	0.50	-	°C/W	
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	1.0		

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static					•	•	ļ
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0$	100	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	-	0.13	-	V/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zara gata valtaga drain aurrant	1	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V		-	-	25	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 17 A <sup>b</sup>	-	-	0.077	Ω
Forward transconductance	9 <sub>fs</sub>	$V_{DS} = 5$	0 V, I <sub>D</sub> = 17 A <sup>b</sup>	8.7	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0  MHz,  see fig.  5		-	1700	-	
Output capacitance	C <sub>oss</sub>			-	560	-	pF
Reverse transfer capacitance	C <sub>rss</sub>			-	120	-	
Total gate charge	Qg			-	-	72	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$I_D = 17 \text{ A}, V_{DS} = 80 \text{ V},$ see fig. 6 and 13 b	-	-	11	
Gate-drain charge	Q <sub>gd</sub>	]	see lig. o and 15	-	-	32	
Turn-on delay time	t <sub>d(on)</sub>			-	11	-	
Rise time	t <sub>r</sub>	$V_{DD}$ = 50 V, $I_{D}$ = 17 A $R_{g}$ = 9.1 $\Omega$ , $R_{D}$ = 2.9 $\Omega$ , see fig. 10 $^{\rm b}$		-	44	-	ns
Turn-off delay time	t <sub>d(off)</sub>			-	53	-	
Fall time	t <sub>f</sub>			-	43	-	
Gate input resistance	$R_g$	f = 1 MHz, open drain		0.5	-	3.6	Ω
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		_	-	28	- A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	110	
Body diode voltage	V <sub>SD</sub>	$T_J = 25  ^{\circ}\text{C},  I_S = 28  \text{A},  V_{GS} = 0  \text{V}  ^{\text{b}}$		-	-	2.5	V
Body diode reverse recovery time	t <sub>rr</sub>	- T <sub>J</sub> = 25 °C, I <sub>F</sub> = 17 A, dl/dt = 100 A/µs b		-	180	360	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	1.3	2.8	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-or			minated b	y L <sub>S</sub> and	L <sub>D</sub> )

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq$  300  $\mu$ s; duty cycle  $\leq$  2 %



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

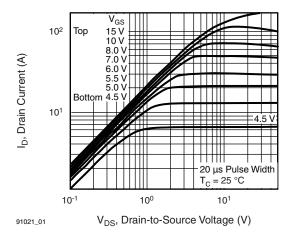


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

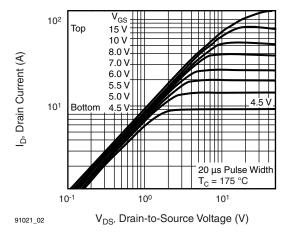


Fig. 2 - Typical Output Characteristics,  $T_C = 175$  °C

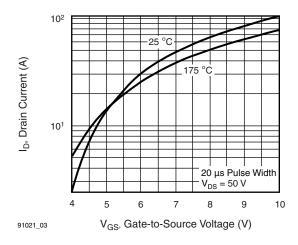


Fig. 3 - Typical Transfer Characteristics

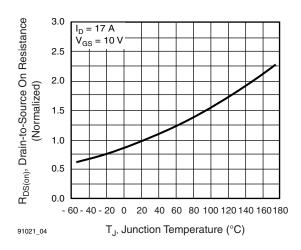


Fig. 4 - Normalized On-Resistance vs. Temperature

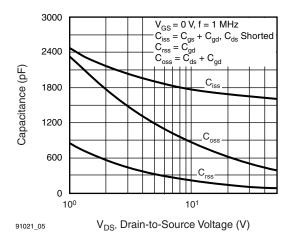


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

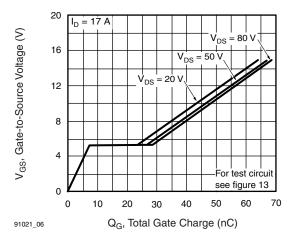


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



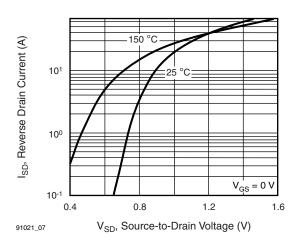


Fig. 7 - Typical Source-Drain Diode Forward Voltage

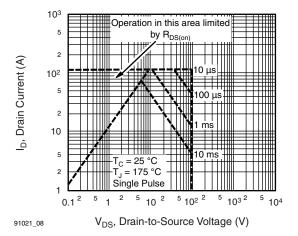


Fig. 8 - Maximum Safe Operating Area

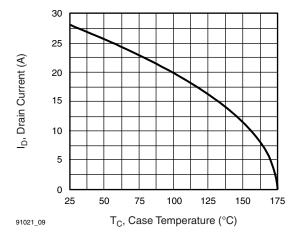


Fig. 9 - Maximum Drain Current vs. Case Temperature

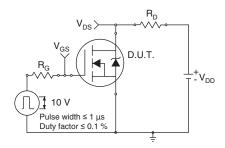


Fig. 10a - Switching Time Test Circuit

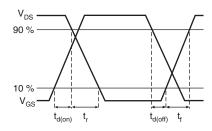


Fig. 10b - Switching Time Waveforms



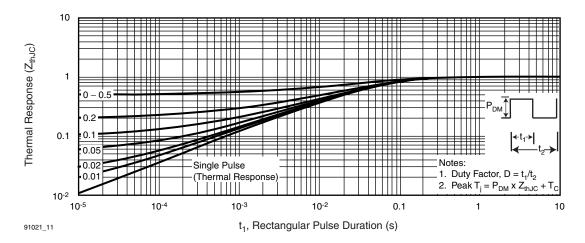


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

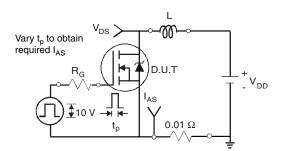


Fig. 12a - Unclamped Inductive Test Circuit

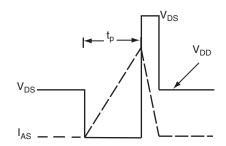


Fig. 12b - Unclamped Inductive Waveforms

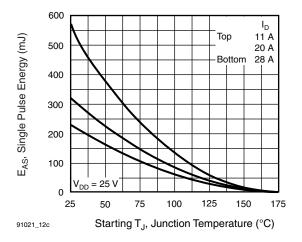
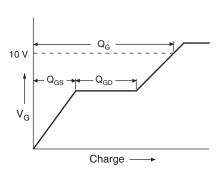
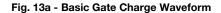


Fig. 12c - Maximum Avalanche Energy vs. Drain Current







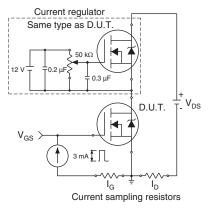


Fig. 13b - Gate Charge Test Circuit

# Peak Diode Recovery dv/dt Test Circuit Circuit layout considerations Low stray inductance Ground plane Low leakage inductance current transformer dv/dt controlled by R<sub>g</sub> Driver same type as D.U.T. I<sub>SD</sub> controlled by duty factor "D" DU.T. - device under test

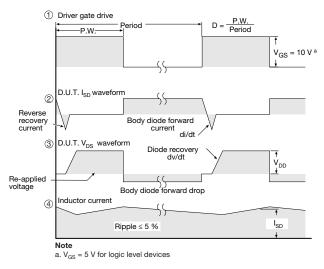


Fig. 14 - For N-Channel

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