SILVACO

Power Architecture e200 Processors

The e200 family of Power Architecture processor cores from Freescale are well proven in a range of embedded applications, including their popular MPC5500 series of automotive MCUs.

The e200 synthesizable, high-efficiency cores are intended for cost-sensitive, embedded real-time applications with significant performance requirements. The two e200 cores available through Silvaco—, e200z1 and e200z6—provide a range of features ideal for automotive, avionics, robotics, industrial control, medical devices, and compact etworking applications.

Built to Power Instruction Set Architecture (ISA) Version 2.03, both cores support variable length encoding (VLE) and implement the full 32-bit Book E instruction set. The cores offer low interrupt latency, AMBA AHB connectivity, and low-power design through clock gating. Debug features include static debug through Nexus Class 1 and real time debug through Nexus Class 2/3.

In addition to running the full 32-bit and VLE instruction sets, the z1 features an MMU for full operating system support. For applications with significant signal processing requirements, the z6 also includes with a seven-stage pipeline machine, a signal processing engine (SPE) and single-precision floating-point unit (FPU), which often eliminates the need for an additional DSP, plus an integrated cache unit.

e200 Family Advanced Features

The e200 cores offer valuable extensions and advanced features while maintaining Power ISA Version 2.03 compatibility and support for PowerPC toolchains.

Variable Length Encoding (VLE)

VLE is a feature developed by Freescale and adopted by Power.org for inclusion in Power ISA Version 2.03. VLE optimizes code density by encoding 32-bit PowerPC instructions into mixed 16 and 32-bit instructions, reducing code footprint by up to 30 percent. 16 and 32-bit instructions may be freely intermixed. VLE is supported by most Power Architecture toolchains and is available on all four of the e200 family cores.

Signal Processing Engine (SPE)

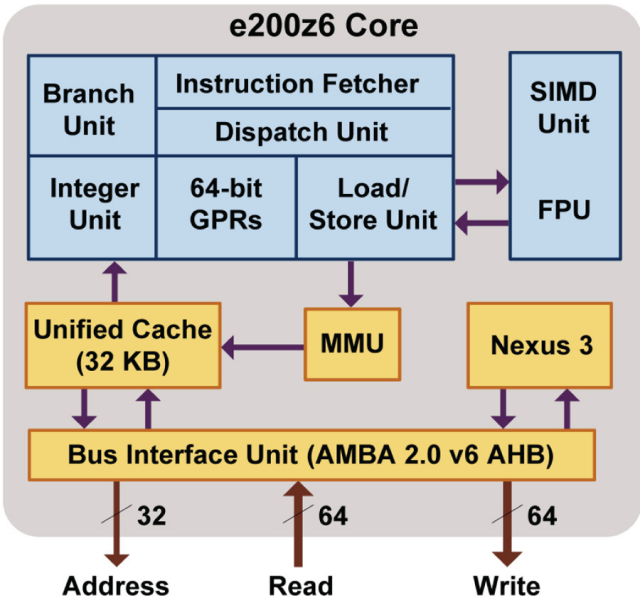
SPE features available on the z6 core provide single-instruction multiple-data (SIMD) operations—execution of one operation on multiple sets of data. On the z6 core, SIMD support is coupled with a floating point unit (FPU) for enhanced DSP operation including 16 and 32-bit integer and fractional data types, signed and unsigned arithmetic, and IEEE single-length floating point operations, with double-precision support available through software.

Memory Management (MMU)

The z1, and z6 cores include an MMU, each with identical functionality and user interface, and cross-core code compatibility. The MMU is ideal for systems that require full operating system support. Its features include:

- Translation from 32-bit effective to 32-bit real addresses:
  - 32-entry MMU in the z6
  - 8-entry MMU in the z1
- Support for nine page sizes (4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, and 256 MB)
- Accesses qualified by:
  - Address spaces: 2 data and 2 instruction
  - 8-bit process identifier (supervisor accessible or global resource)
- Selectable access privileges:
  - User Read/Write/Execute (UR/UW/UX)
  - Supervisor Read/Write/Execute (SR/SW/SX)

e200z6 Core Features

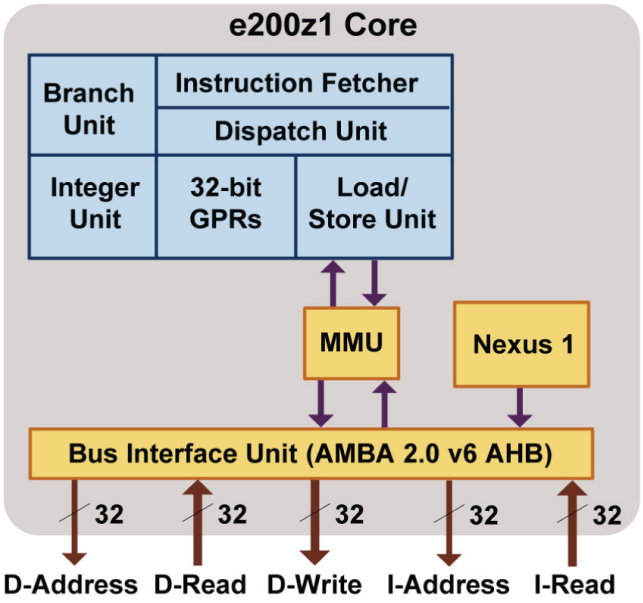


The z6 core is the high-end member of the e200 core family and offers the following features:

- 7-stage pipeline with in-order execution
- Single-issue (one instruction issued per clock cycle)
- 32-bit Power Architecture Book E CPU core

- VLE for code density
- Unified 32-KB, 8-way set-associative cache
- 32-entry unified MMU
- SIMD and FPU for enhanced DSP support
- AMBA AHB 2.0 v6 bus interface
- Single-cycle execution for most instructions
- Integer and floating point multiply and multiply-accumulate in 3 clocks, fully pipelined
- Integer divide in 6 to 16 clocks, unpipelined
- 3-cycle loads
- 1 to 3-cycle branches
- Small branch target address cache (BTAC) to accelerate loops
- Nexus Class 3 support

e200z1 Core Features



The z1 core is ideal for cost-sensitive applications that require an MMU but do not need enhanced DSP support. It offers:

- Single-issue, in-order, 4-stage pipeline
- 32-bit Power Architecture Book E CPU core
- VLE for code density
- 8-entry unified MMU
- AMBA AHB 2.0 v6 bus interface
- Single-cycle execution for most instructions
  - 1-cycle load, store, arithmetic, logical, and multiply
  - 1 to 2-cycle branches
  - Integer divide 6 to 16 clocks (unpipelined)
- Nexus Class 1 support

Feature	e200z1	e200z6
Architecture	Power ISA 2.03 (32-bit)	Power ISA 2.03 (32-bit)
Book E ISA	Yes	Yes
VLE	Yes	Yes
L1 Unified Cache	—	32-KB, 8-way
MMU	8-entry	32-entry
SPE	—	64-bit
FPU	—	32x32
Bus Interface	Dual AMBA 2.0 v6 32-bit read 32-bit write 32-bit address	Single AMBA 2.0 v6 64-bit read 64-bit write 32-bit address

Deliverables

- Synthesizable Verilog source code
- Integration testbench
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

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