DATA SHEET

凌陽科技
SUNPLUS

SPCA718A

SVCD Decoder

Preliminary

MAR. 11, 2002

Version 0.1

Table of Contents

PAGE

SVCD DECODER

1. GENERAL DESCRIPTION

The SPCA718A A/V decoder is a high-performance low-cost single-chip SVCD decoder. It performs real-time decoding and playback of ISO/IEC 13818/11172 MPEG2/MPEG1 data stream.

The SPCA718A is extremely superior in SVCD and VCD application system. It utilizes the least external memory to build a complete SVCD/VCD player. In the SVCD case, it requires only one 1Mx16 SDRAM and one 256kx8 ROM, whereas in the VCD system, it requires only one 1Mx16 SDRAM or 256Kx16 EDO DRAM and one 256kx8 ROM. For enhanced applications it can extend external SDRAM from 16Mbits to 128Mbits and EDO DRAM from 4M bits to 32M bits.

The SPCA718A combines all the functions necessary for a typical SVCD system, such as a house-keeping RISC, efficient MPEG audio/video decoder, DRAM controller, on screen display, an embedded high resolution ADC and stereo key controller for Karaoke. The SPCA718A also includes a flexible programmable interface and allows the application engineer to further expand SVCD functionality. With this interface, the system developer can greatly expand SVCD system capability.

The SPCA718A is designed to connect to standard TV encoder, audio DAC(s), and CD-DSP without glue logic.

A sample system utilizing the SPCA718A is presented below:

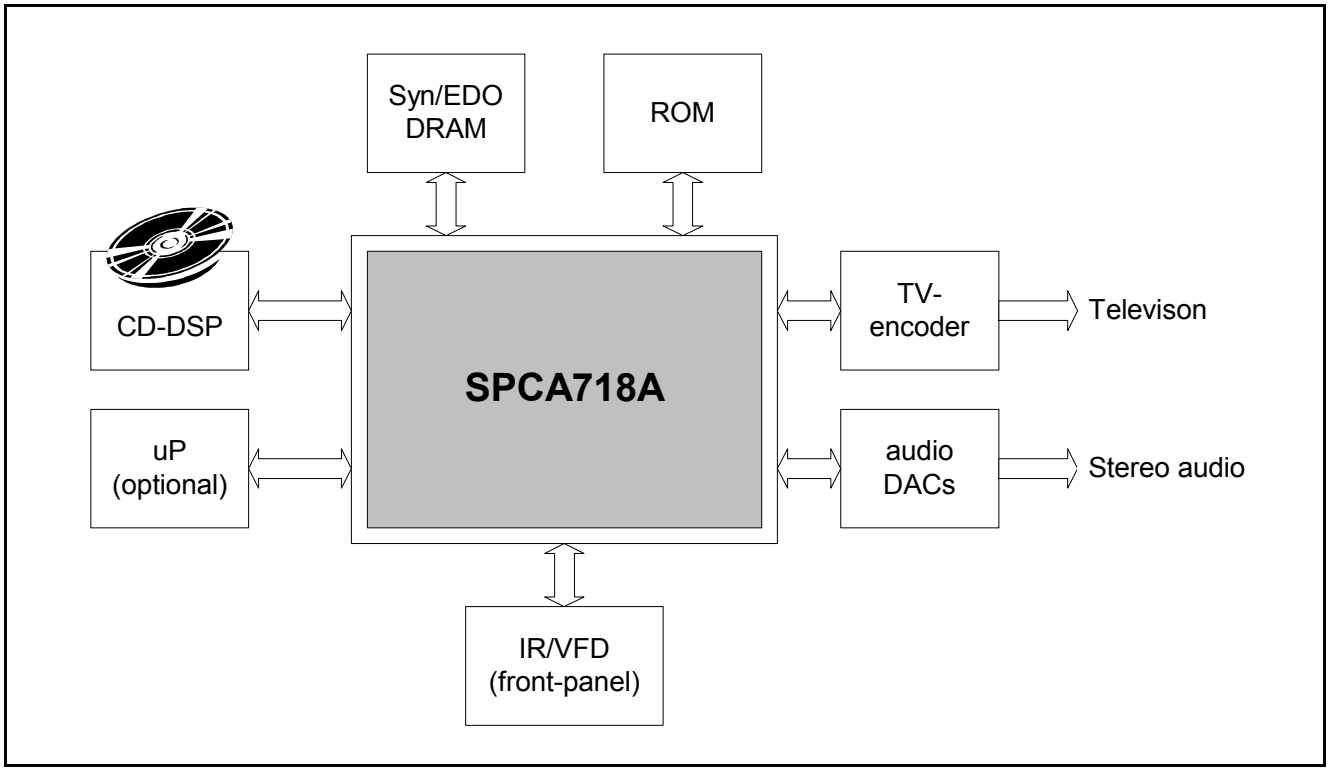


Figure 1-1 SVCD System Block Diagram

2. FEATURES

2.1. General Features

1.) SVCD/VCD/CD compatibility
2.) CD-DSP interface
3.) Supports 1Mx16 bits SDRAM, up to 128M bits
4.) Supports 256Kx16 bits EDO DRAM, up to 32M bits
5.) Supports 256kx8 bitsROM, up to 3x256M bits ROM/flash
6.) Power control mode
7.) Glueless interface to SDRAM, EDO DRAM ROM, Audio DAC, CD-DSP and TV encoder

2.2. System

Real time MPEG1 system stream program stream parsing and de-multiplexing

2.3. Real time video decompression

1.) Decode ISO/IEC 11172-2/13818-2 video bitstream
2.) Decode MPEG1/MPEG2 video up to 704x576/720x576
3.) Programmable hybrid video error concealment

2.4. Real Time Audio Decompression And Playback

1.) MPEG audio layer 1 and 2 decompression conforming to ISO 11172-3/13818-3 standard
2.) Automatic audio error concealment
3.) Digital volume control
4.) Key control function
5.) Advanced sound effects
6.) Built-in A/D converter for Karaoke
7.) FU-DU function for language and song learning
8.) Karaoke scoring function
9.) Microphone silence detection
10.) Equalization function

2.5. Advanced Video Processing And Display

1.) Supports NTSC and PAL TV standards
2.) Perform vertical scaling to allow NTSC/PAL source to be displayed on PAL/NTSC TV in correct aspect ratio
3.) Performs real time processing at 352x240x30 fps 352x288x25 fps, 480x480x30 fps and 480x576x25 fps
4.) Horizontal and Vertical Interpolation for high quality video output
5.) OGT conforms to SVCD standard to support mult-language subtitle

2.6. 4 Bit OSD

Video fade-in/fade-out

2.7. Versatile Programmable Interface

1.) Supports UART to connect to HOST RS232 port
2.) Supports parallel mode host control interface
3.) Supports programmable serial I/O interface for IR in/out and VFD control, etc.

2.8. Special Graphic And Audio Architecture For Game And Education Program Development

2.9. Built-In Plls Generate System And Audio Clocks

2.10. JPEG Decoding Capability To Support High Resolution Still Picture Decoding

2.11. Software Drivers

1.) Drivers for CD-I (green book, white book), Karaoke CD, Video CD 2.0/1.1 and Audio CD (CD-DA)
2.) Preview
3.) User definable features
4.) ZoomPro: Programmable video Zoom-in/out
5.) ImagePro: Programmable digital image processing

2.12. Component Features

1.) Supply voltage: 2.5 volts (kernel), 3.3 volts (I/O)
2.) I/O interface: 5 volts tolerance
3.) Package: 128/160-pin QFP

3.BLOCK DIAGRAM

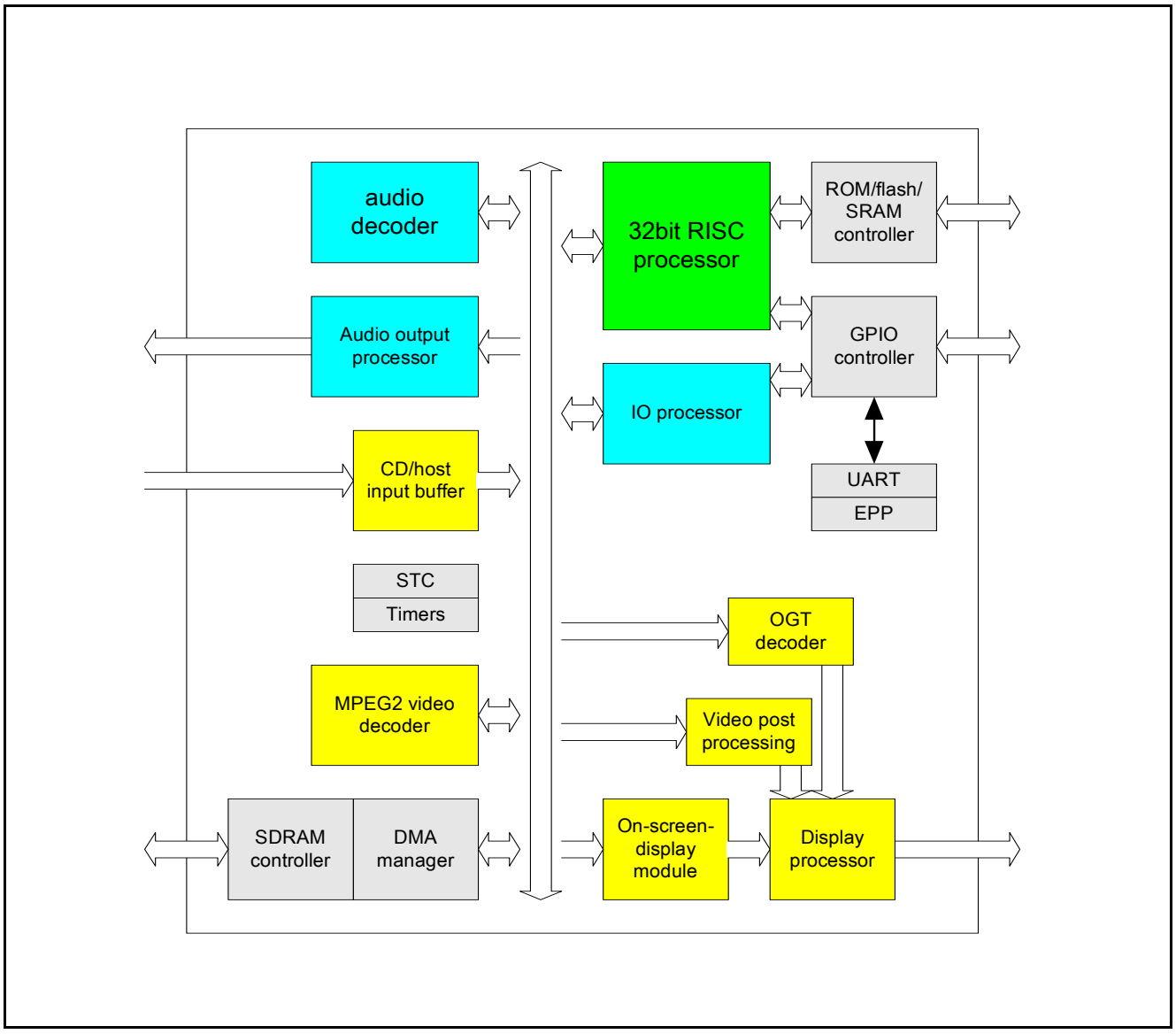


Figure 3-1 SPCA718A Block Diagram

4.SIGNAL DESCRIPTIONS

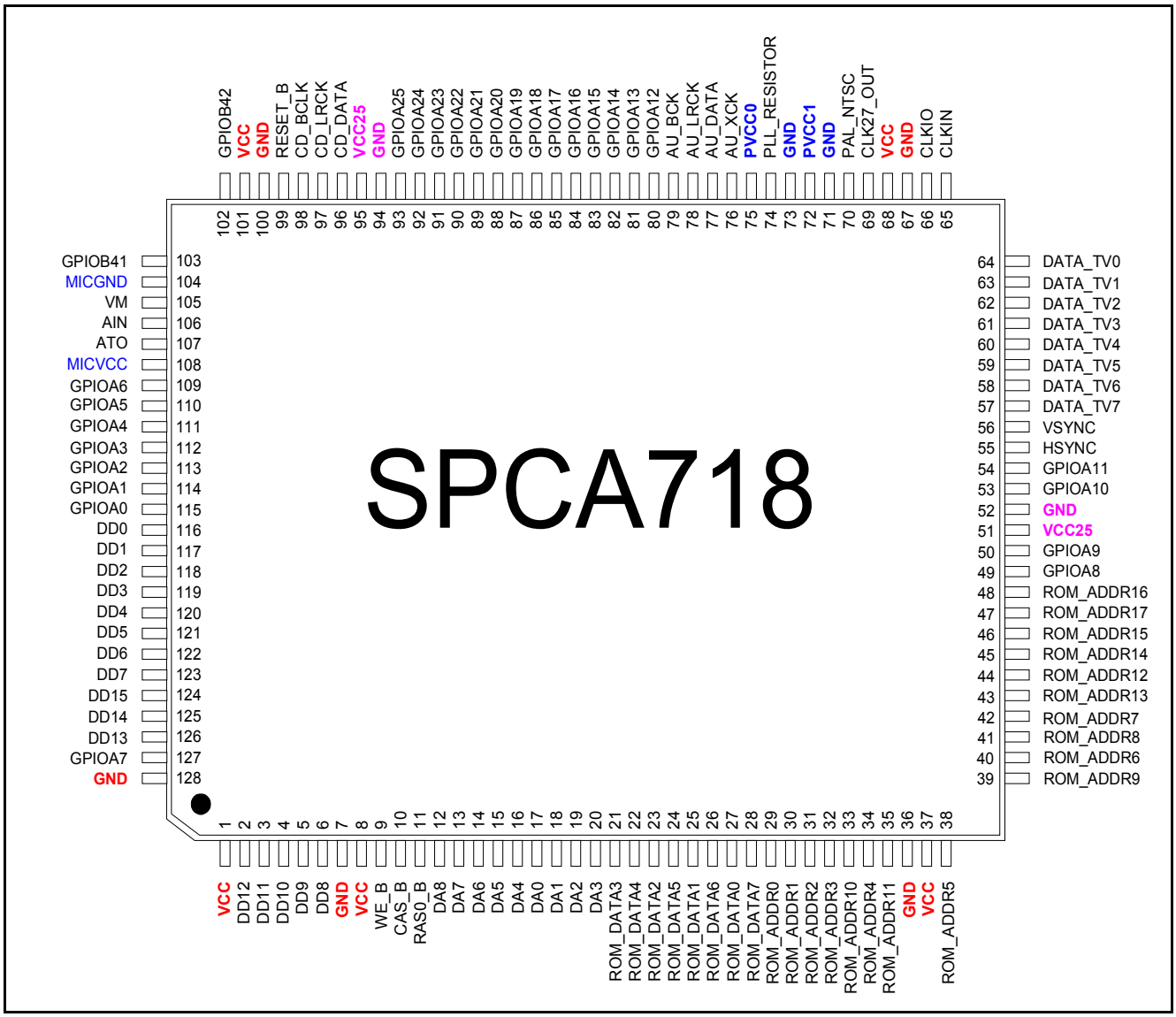


Figure 4-1 SPCA718A Pin Map

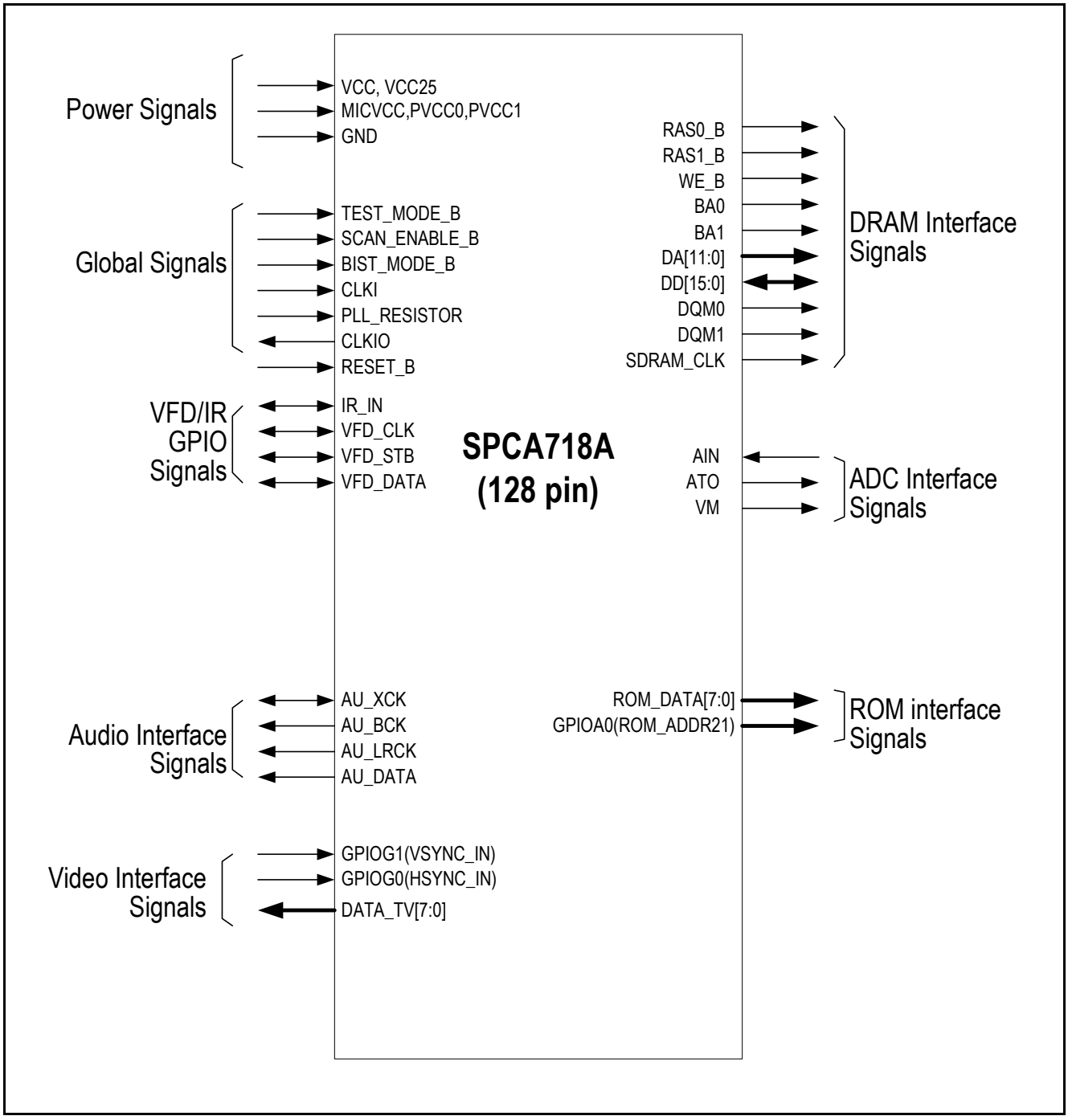


Figure 4-2 SPCA718A Signal Group Map

4.1. Signal Descriptions

Table 4-1

SDRAM/EDO RAM Interface		
PIN	**Direction**	**Description**
DD[15:0]	I/O	DRAM data bus
DA [11:0]	O	DRAM address bus
RAS0_B	O	RAS strobe for first DRAM
RAS1_B	O	RAS strobe for second DRAM
CAS_B	O	CAS strobe for SDRAM
WE_B	O	Write enable for SDRAM
DQM0	O	DQM should be connected to LDQM & UDQM of SDRAM, DQM for first SDRAM
DQM1	O	DQM for second SDRAM
BA0	O	Bank select 0 of SDRAM
BA1	O	Bank select 1 of SDRAM
SDRAM_CLK	O	Clock for SDRAM

Table 4-2

Clock & Reset Interface		
PIN	**Direction**	**Description**
CLKIN	I	27MHz clock input or connect to crystal
CLKIO	O	
RESET_B	I	Device reset pin, active LOW

Table 4-3

Audio Interface		
PIN	**Direction**	**Description**
AU_DATA	O	Audio data output
AU_LRCK	O	Audio left/right clock
AU_XCK	I/O	Audio clock
AU_BCK	O	Audio bit clock for PCM

Table 4-4

ADC Interface		
Pin	**Direction**	**Description**
VM	O	Reference voltage for ADC
AIN	I	Negative input of ADC
ATO	O	Microphone amplifier output

Table 4-5

PLL Interface		
PIN	**Direction**	**Description**
PLL_RESISTOR	I	External resistor for PLL circuit

Table 4-6

ROM/Flash Interface		
PIN	**Direction**	**Description**
ROM_DATA[7:0]	I/O	Data bus bit 7 to bit 0 for ROM/flash
ROM_ADDR[19:0]	O	Address bus bit 19 to bit 0 for ROM/flash The extended address bus bit 18, 19 is provided through GPIOA[8] and GPIOA[9]

Table 4-7

TV encoder Interface		
PIN	**Direction**	**Description**
DATA_TV[7:0]	O	Video output
HSYNC	I	Horizontal sync
VSYNC	I	Vertical sync

4.2. Hardware Configuration

PIN	**Description**			
ROM_ADDR[0]	hardware configuration : Default Mode			
Set the default configuration	0		1	
	CK_SEL, TEST_MODE are controlled by ROM_ADDR[4:1]		CK_SEL = 2'b11 TEST_MODE = 2'b11	
ROM_ADDR[2:1]	hardware configuration : CK_SEL[1:0]			
Set system clock frequency	2'b11	2'b10	2'b01	2'b00
	54 MHz	67.5 MHz	81 MHz	40.5 MHz
ROM_ADDR[4:3]	Hardware configuration : TEST_MODE[1:0]			
Normal Mode should be selected	2'b11	2'b10	2'b01	2'b00
	Normal	PLL Bypass	BIST Test	SCAN test

4.3. Multifunction Pin List

All multifunction pins are controlled by register GPIO_SEL and GPIO_SEL_AUX.

GPIOA[0]	GPIO_SEL[1:0]				BIST_MODE	RST
	2'b00	2'b01	2'b10	2'b11		
	GPIOA[0]	RAS1_B	BA1	NC	ADC_S[0](I)	GPI
GPIOA[1]	GPIO_SEL[2]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[1]		DQM0		ADC_S[1](I)	GPI
GPIOA[2]	GPIO_SEL[3]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[2]		DQM1		ADC_S[2](I)	GPI
GPIOA[3]	GPIO_SEL[2]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[3]		BA0		ADC_PWAD(I)	GPI

	GPIO_SEL[5:4]				BIST_MODE	RST
	2'b00	2'b01	2'b10	2'b11		
GPIOA[4]	GPIOA[4]	DA[9]	DA[9]	DA[9]	ADC_MCLK(I)	GPI
GPIOA[5]	GPIOA[5]	GPIOA[5]	DA[10]	DA[10]	ADC_FS(I)	GPI
GPIOA[6]	GPIOA[6]	GPIOA[6]	GPIOA[6]	DA[11]	ADC_SPGA(I)	GPI
GPIOA[7]	GPIO_SEL[6]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[7]		SDRAM_CLK		NC	GPI
GPIOA[8]	GPIO_SEL[7]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[8]		ROM_ADDR[18]		BIST_FAIL	ROM_ADDR[18]
GPIOA[9]	GPIO_SEL[8]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[9]		ROM_ADDR[19]		NC	ROM_ADDR[19]
GPIOA[10]	GPIO_SEL[9]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[10]		SDATA		ADC_D[0](O)	GPI
GPIOA[11]	GPIO_SEL[9]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[11]		SCL		ADC_D[1](O)	GPI
GPIOA[12]	GPIO_SEL[11:10]				BIST_MODE	RST
	2'b00	2'b01	2'b10	2'b11		
	MEMOE_B	AU_DATA2	GPIOA[12]	NC	ADC_D[2](O)	MEMOE_B
GPIOA[13]	GPIO_SEL[12]				BIST_MODE	RST
	1'b0		1'b1			
	MEMWE_B		GPIOA[13]		ADC_D[3](O)	MEMWE_B
GPIOA[14]	GPIO_SEL[13]				BIST_MODE	RST
	1'b0		1'b1			
	GPIOA[14]		NC		ADC_D[4](O)	GPI
GPIOA[15]	GPIO_SEL[14]				BIST_MODE	RST
	1'b0		1'b1			
	MEMCS3_B		GPIOA[15]		ADC_D[5](O)	MEMCS3_B
	GPIO_SEL[15]				BIST_MODE	RST
	1'b0		1'b1			
GPIOA[16]	MEMCS1_B		GPIOA[16]		ADC_D[6](O)	MEMCS1_B
GPIOA[17]	MEMCS2_B		GPIOA[17]		ADC_D[7](O)	MEMCS2_B
	GPIO_SEL_AUX[0]				BIST_MODE	RST
	1'b0		1'b1			
GPIOA[18]	GPIOA[18]		UA_TXD		ADC_D[8](O)	GPI
GPIOA[19]	GPIOA[19]		UA_RXD		ADC_D[9](O)	GPI
	GPIO_SEL_AUX[1]				BIST_MODE	RST
	1'b0		1'b1			
GPIOA[20]	GPIOA[20]		UA_RTS_B		ADC_D[10](O)	GPI
GPIOA[21]	GPIOA[21]		UA_CTS_B		ADC_D[11](O)	GPI

	GPIO_SEL_AUX[2]		BIST_MODE	RST
	1'b0	1'b1		
GPIOA[22]	GPIOA[22]	UA_DTR_B	ADC_D[12](O)	GPI
GPIOA[23]	GPIOA[23]	UA_DSR_B	ADC_D[13](O)	GPI
GPIOA[24]	GPIOA[24]	UA_DCD_B	ADC_D[14](O)	GPI
GPIOA[25]	GPIOA[25]	UA_RI_B	SPT_IN(I)	GPI
	GPIO_SEL_AUX[3]		BIST_MODE	RST
	1'b0	1'b1		
HSYNC	HSYNC	GPIOA[28]	NC	HSYNC
VSYNC	VSYNC	GPIOA[29]	NC	VSYNC
	GPIO_SEL_AUX[4]		BIST_MODE	RST
	1'b0	1'b1		
DATA_TV[7]	GPIOA[37]	DATA_TV7	SPT_OA(O)	GPI
DATA_TV[6]	GPIOA[36]	DATA_TV6	SPT_OB(O)	GPI
DATA_TV[5]	GPIOA[35]	DATA_TV5	SPT_OC(O)	GPI
DATA_TV[4]	GPIOA[34]	DATA_TV4	SPT_OSC(O)	GPI
DATA_TV[3]	GPIOA[33]	DATA_TV3	NC	GPI
DATA_TV[2]	GPIOA[32]	DATA_TV2	NC	GPI
DATA_TV[1]	GPIOA[31]	DATA_TV1	NC	GPI
DATA_TV[0]	GPIOA[30]	DATA_TV0	NC	GPI
CLK27_OUT	GPIO_SEL_AUX[5]			RST
	1'b0	1'b1		
	GPIOA[38]	CLK27_OUT		GPI
PAL_NTSC	GPIO_SEL_AUX[6]			RST
	1'b0	1'b1		
	GPIOA[39]	PAL_NTSC		GPI
IOP_NMI from (set to GPI first)	GPIO_SEL_AUX[11:10]			
	2'b00	2'b01	2'b10	2'b11
	0	GPIOA[14]	GPIOA[13]	GPIOA[9]
RISC Interrupt	Select	1'b1		1'b0
Interrupt[3]	GPIO_SEL_AUX[12]	GPIOA[9]		0
Interrupt[4]	GPIO_SEL_AUX[13]	GPIOA[13]		0
Interrupt[5]	GPIO_SEL_AUX[14]	GPIOA[14]		0
Interrupt[6]	GPIO_SEL_AUX[15]	GPIOA[15]		0

5.FUNCTIONAL DESCRIPTIONS

5.1. System Sync

5.1.1. Some abbreviations for system sync module

STC System Time Clock
SCR System Clock Reference
DTS Decode Time Stamp
PTS Presentation Time Stamp
STD System Target Decoder (ideal decoder)
PU Presentation Unit
AU Access Unit
DSM Digital Storage Medium
Fs Sampling Frequency

5.1.2. Timers and time stamps

5.1.2.1. System time clock (STC)

The System Time Clock is the main clock counter used for all time references. The STC is a 33-bit counter based on a 90kHz clock.

5.1.2.2. System clock reference (SCR)

The System Clock Reference is a time stamp in the MPEG system stream. The SCR value represents the time when the last byte of the SCR field leaves the encoder. For the decoder, this value is used to initialize the STC and for updating the STC when using the DSM as time master.

5.1.2.3. Decode time stamp (DTS)

The Decode Time Stamp value represents the time when an access unit should be ready for decoding. For the Audio stream, the DTS == PTS so it is not used. In the Video stream, the DTS for I-Frames and P-Frames are nominally equal to the PTS value minus the number of picture periods of video reordering delay multiplied by the picture period, in units of the 90kHz STC.
Presentation Time Stamp (PTS)

5.1.2.4. Presentation time stamp (PTS)

A Presentation Time Stamp represents the time at which a presentation unit should be displayed. In the case of Audio, this is the time when the decoder should begin the playback of an audio frame. In the case of Video, this is the time when the corresponding video frame should be displayed.

5.1.3. Time master

A decoding system, including all of the synchronized decoders and the source of the coded data, must have exactly one independent time master. The SPCA718A chip allows the microcode to use either the DSM or Audio block as the time master. The time master selection is implied by how the STC is updated.

5.1.3.1. DSM as time master

To use the Digital Storage Medium, in this case the Video CD reader, as the time master, follow the following synchronization guidelines:

1.) Initialize the STC to the first SCR received.
2.) Set the STC to run (incrementing at 90kHz).
3.) Maintain the STC by updating it with SCR values received.
4.) Video presentations are made when the video PTS==STC.
5.) Audio presentations are made when the audio PTS==STC.

5.1.3.2. Audio as time master

To use the Audio block as the time master, follow the following synchronization guideline:

1.) Initialize the STC to the first SCR received.
2.) Set the STC to run (incrementing at 90kHz)
3.) Maintain the STC by updating it with Audio PTS values received.
4.) Video presentations are made when the video PTS==STC.
5.) Use SRC values to determine if the DSM data rate is correct.

5.2. Video Decoder

The Video Decoder of SPCA718A is an MPEG-2 video decoder optimized for minimum cost while conforming to ISO 13818-2 standard. The module will read a MPEG video stream in and continuously reconstruct video frames to external DRAM. Then a video processor will process the generated video frames and prepare for video display. The Video Decoder performs the following functions:

1.) Huffman Decoding
2.) Inverse Quantization
3.) Inverse Cosine Transform
4.) Motion Vector Generation
5.) Address Generation
6.) Motion Compensation

5.3. Video Processor

The Video Processor & Output Interface is responsible for taking decompressed data from memory (DRAM) and processing the data into raster (interlaced or non-interlaced) video. Some of the important processing functions include horizontal/vertical interpolation, filtering and clipping.

The video processing functions performed by the video processor include vertical interpolation, horizontal interpolation, horizontal filtering, proprietary high-resolution functions and clipping functions. Video interpolations allow for small SIF images of MPEG video decoding to be enlarged without blocky or

discontinuity effects. The final display of the SIF image will have smooth transitions in both horizontal and vertical directions. Horizontal filtering will also be performed to reduce any alias effects. The proprietary high-resolution functions are used to maintain quality in the 704 X 576 high resolution still image mode. Clipping function can be turned on to allow for compatibility with CCIR 601 specifications.

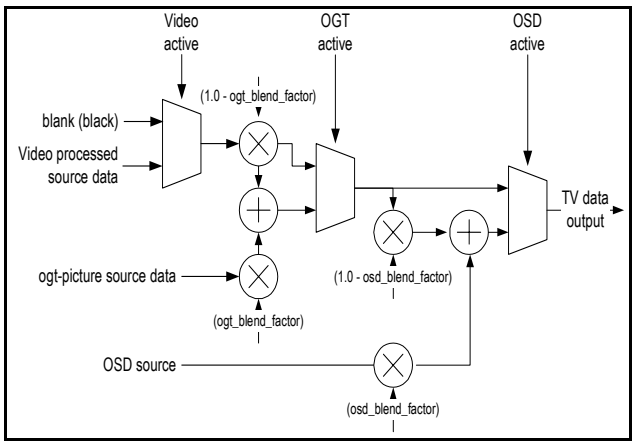


Figure 5-1 Video Processor Output Mixer

5.3.1. Video processor interface

The SPCA718A can support the ITU-R 601 or 656 standard TV encoder interface. The I/O interface of the video processor is defined below:

HSYNC Horizontal sync Input
Horizontal sync signal inputted from the TV encoder.
VSYNC Vertical sync Input
Vertical sync signal inputted from the TV encoder.
DATA_TV(7:0) Video out Output
These pins are the video data output bus. They contains multiplexed Luminance and Chrominance video data.
PAL_NTSC PAL/NTSC control Output
This pin controls the PAL/NTSC mode of the TV encoder.

The recommended interface scheme for 601 is shown in Figure 5-2 below:

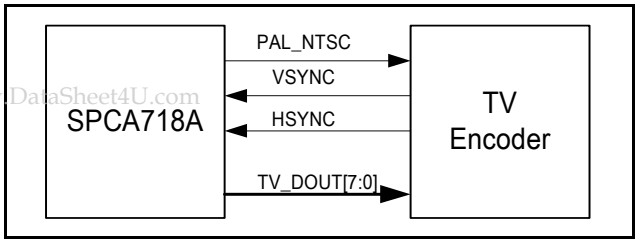


Figure 5-2 TV encoder interface (601)

5.3.2. Usage for 8 bit video interface

SPCA718A co-operates with master-mode TV-encoders. When operate at 601 mode, VSYNC and HSYNC signals come from a standard TV-encoder (as in figure 5-2.) SPCA718A will lock to these reference timing and output the data onto the DATA_TV[7:0]. The data is sequenced out after HSYNC_IN falling edge using time-multiplexed 4-2-2 format (2 chroma samples for 4 luma samples.). Detailed timing diagram of TV encoder interface is presented in Figure 5-3 below:

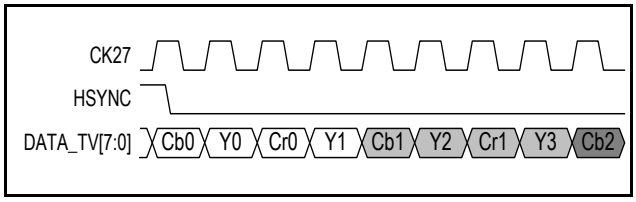


Figure 5-3 8 bit Video Interface Timing

5.4. On Screen Display

The on screen display (OSD) function of the SPCA718A provides users with overlay bitmap graphics on the final TV display. Applications can use this feature to display specific information such as disc remaining time or other status of the player.

The SPCA718A supports 4, 16 or 256 indexed color which provide link-list OSD region management so that the application can display several independent regions with different color tables. The Host or RISC will program these headers and data then store to the DRAM for a variety of purposes. OSD decoder reads these header and data, then interpret to be a graphic data and overlaid with video to be output to the display device.

For every OSD region there is a header field associated with it. The header will provide OSD decoder information to interpret the succeeding bit mapped data.

5.4.1. Link address

This address shows the address of next OSD region and OSD decoder use it to next OSD block in the DRAM. Figure 5-4 shows the linked list structure.

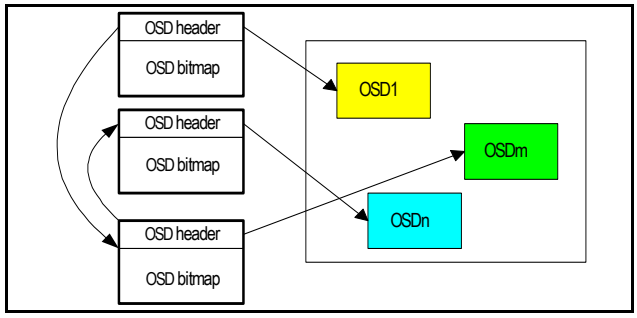


Figure 5-4 Link List Structure

5.4.2. Start row address

This address indicates the start vertical address of bitmapped data begin to display on the screen.

5.4.3. Start column address

This address indicates the start horizontal address of bitmapped data begin to display on the screen.

5.4.4. HSIZE

This parameter gives the width of the associated OSD region.

5.4.5. VSIZE

This parameter gives the height of the associated OSD region.

5.4.6. Color table update

If this bit is active, there will be a color look-up table following the header. The luminance part, Y, is represented by 6 bits and the chrominance part , Cb and Cr, are represented by 4 bits each. The bitmapped data following the OSD header are 2 bits per pixel.

5.4.7. Blend level

This parameter gives the ratio of OSD that will mix with the corresponding video data to be displayed on the screen.

5.5. Audio Decoder

The SPCA718A audio decoder is capable of decoding various audio formats. These formats includes:

— MPEG1 Layer-1 and Layer-2

In addition the SPCA718A audio decoder can provide advanced audio-processing and apply special sound-effects to selected channels. These sound effects include:

1.) Key control (for karaoke function)
2.) Advanced sound-field processing
3.) Advanced adjustable echo effect

5.6. Audio Output Interface

The Audio Output Interface takes PCM data from memory (DRAM) and outputs it in bit-serial format to external audio DACs. The PCM audio data will be in alternating left/right channel format if the data is in the stereo mode. In the mono mode, the data will be a list of PCM values.

5.6.1. Audio output interface signals

The signals from the Audio Output Interface is as follows:

AU_DATA Audio data bus Output
Serial audio data clocked out relative to AUD_BCK.

AU_LRCK Audio Left/Right clock Output
Left/Right data channel indicator.

AU_BCK Audio bit clock Output
Audio bit clock output. Depending on audio output mode, this signal can be derived from the master clock or be AUD_XCK divided by 8. It can be either 48 or 32 times the sampling clock.

AU_XCK External audio clock Input
When the SPCA718A is programmed for external audio clock mode, the audio clock will come from this signal. When programmed for internal audio clock, this signal will reflect the internal audio clock.

A typical connection scheme is shown in Figure 5-5 below:

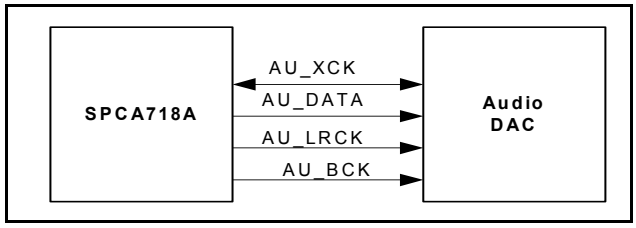


Figure 5-5 Audio Output Interface

A timing diagrams of the audio interface clocking modes are presented in Figure 5-6 below.

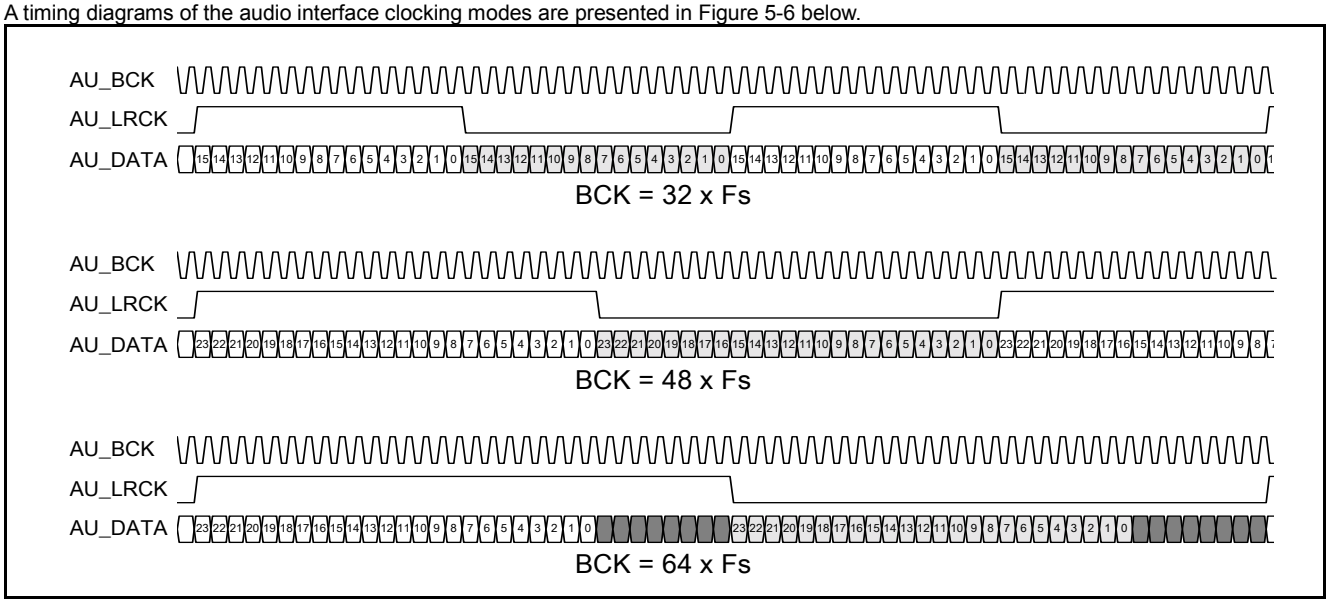


Figure 5-6 Some Audio Interface Clocking Modes

5.7. Dram Interface

The DRAM interface is used by the SPCA718A to access DRAM for all required functions in the system including bit stream storage after parsing, reading bit stream into the Video Decoder hardware, Video Decoder reference read and reconstructed write, Video Processor display data read, OSD data store and read, etc.

5.7.1. Dram timing

The DRAM interface is designed to work with 1Mx16/ 4Mx16 SDRAM or 256Kx16 EDO DRAM. The SPCA718A efficiently uses most memory bandwidths to save power and run in a lower frequency. Figures 5-7and 5-8 provide sample timing diagrams.

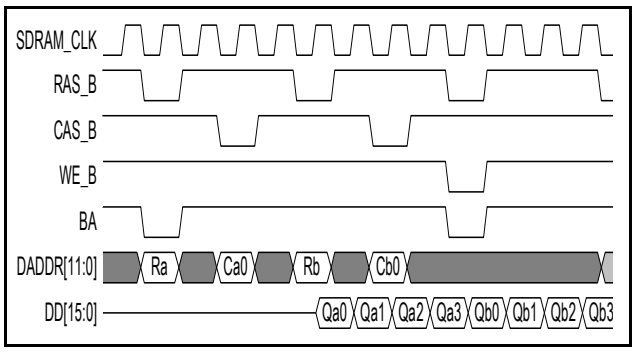


Figure 5-7 SDRAM Read Timing

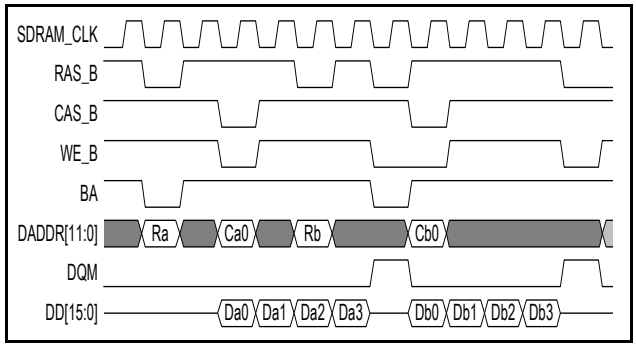


Figure 5-8 SDRAM Write Timing

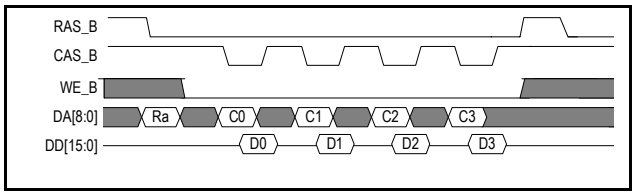


Figure 5-9 EDO DRAM Read Timing

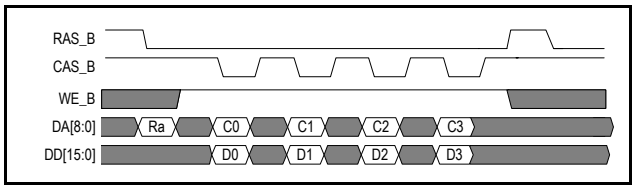


Figure 5-10 EDO DRAM Write Timing

DRAM refresh cycle is supported using standard SDRAM refresh cycle. This eliminates the need for a refresh address counter. The frequency of refresh is programmable.

5.7.2. DRAM memory map

Figure 10-4 shows the DRAM memory map of the SPCA718A. The memory is partitioned into several regions. These regions are as follows:

1.) System buffer
2.) IOP buffer
3.) Audio work buffer
4.) Audio echo buffer
5.) OSD Buffer
6.) CD Buffer
7.) Video bitstream buffer
8.) Audio bitstream buffer
9.) Reference Frame0 of Luminance
10.) Reference Frame0 of Chrominance
11.) Reference Frame1 of Luminance
12.) Reference Frame1 of Chrominance
13.) B Frame of Luminance
14.) B Frame of Chrominace

A programmable pointer points to each region. The RISC can change the content of these pointers via register files.

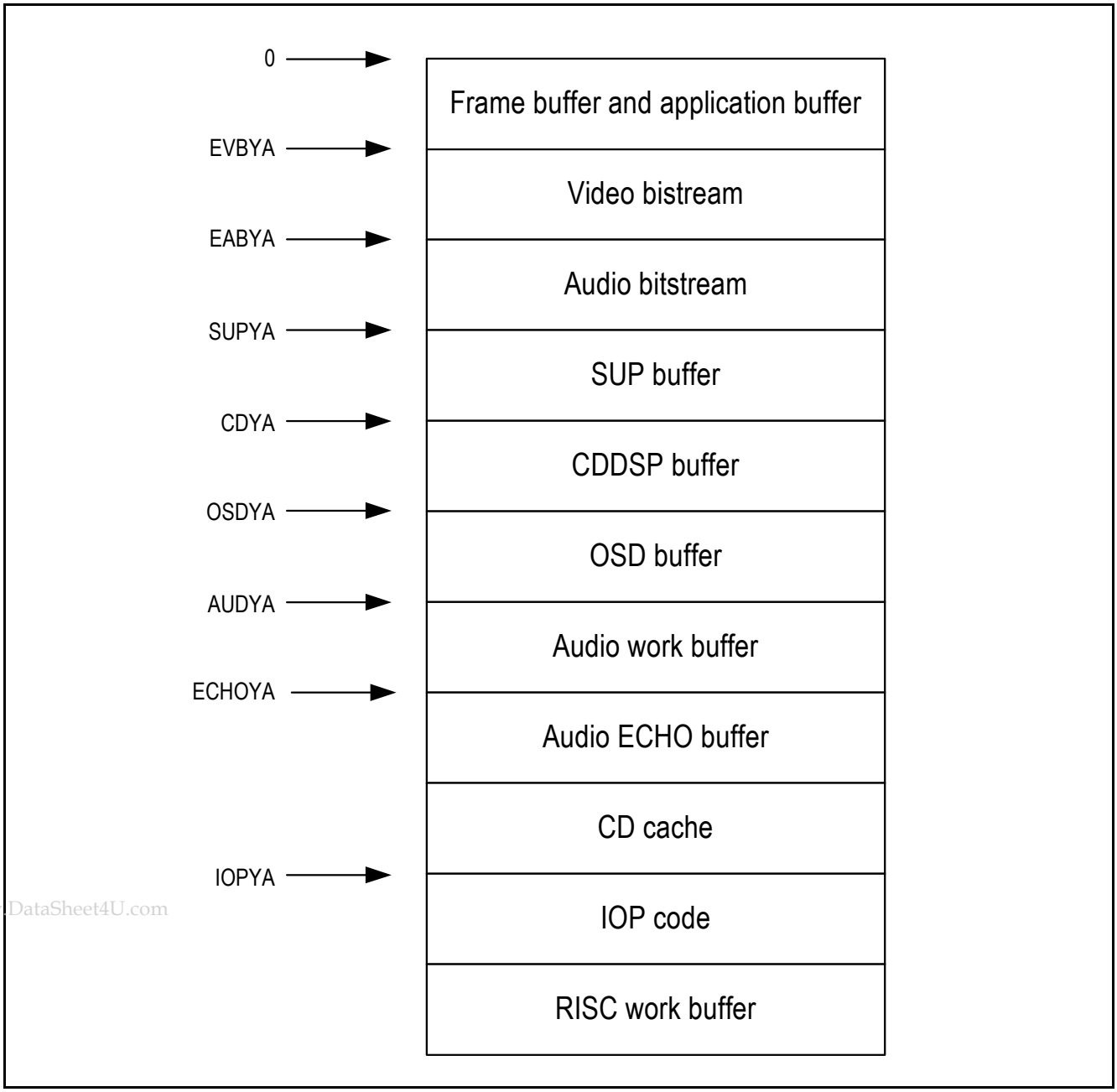


Figure 5-11 DRAM memory mapping

5.8. Rom/Flash Interface

The SPCA718A provides flexible connections to external ROM, Flash or SRAM. It can support up to 3 discrete ROM memory spaces by using different chip-selects (*ROM_CS1 ~ CS3*). Every memory space can be in different wait-state setting.

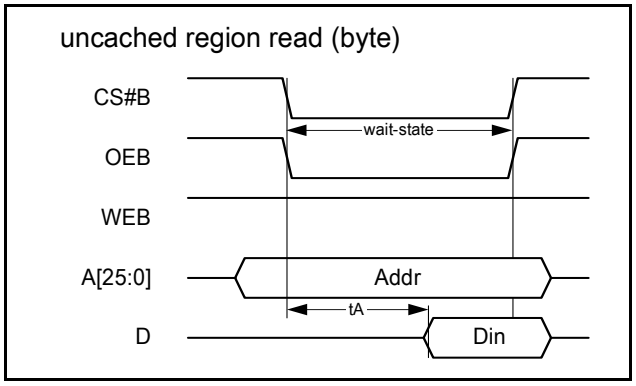


Figure 5-12 Uncached region read

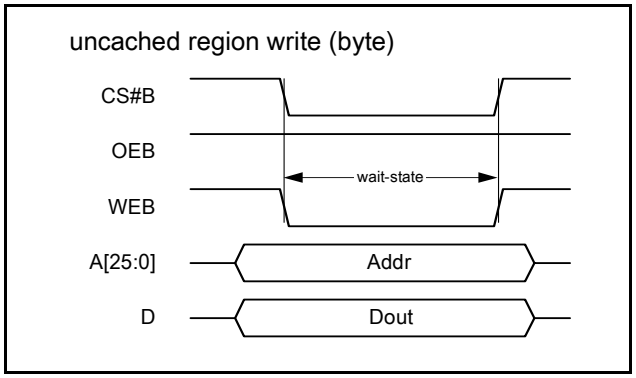


Figure 5-13 Uncached region write (for SRAM or flash program)

5.9. CD Interface

The CD interface is a simple serial interface for standard CD-DSPs. Serial data from the CD-DSP is shifted into the SPCA718A, preprocessed by the CD interface module, then written to DRAM for post-processing by the RISC processor. Since post-processing is accomplished by the RISC processor, the data stream can be in any format. For example: CD-DA, CD-ROM, CD-ROM/XA, CD-I, MPEG1 system streams, MPEG1 video streams and MPEG1 audio streams. Note that in the CD-DA format, since no post-processing is necessary, the serial data can be routed directly to the audio DACs.

The RISC processor and dedicated hardware is responsible for the following CD data stream post-processing functions when the data format is not CD-DA :

1.) Real-time parsing for Mode 2 form 2 sectors.
2.) Real-time parsing for Mode 1 and Mode 2 form 1 sectors (including error correction when not decoding MPEG).
3.) Real-time processing of Mode 0 and skipping to next sector.
4.) Q-erasure correction, P-erasure correction and P-error check.

Notice that the preprocessed serial data can be routed directly to the Audio output stage for CD-DA format data or stored in DRAM for post-processing.

The CD interface is composed of the following signals:

CD_DATA CD serial data Input

Serial data input from the CD-DSP:

CD_LRCK CD Left/Right Clock Input

CD_LRCK provides 16-bit word synchronization to the SPCA718A and has several programmable features, such as polarity, delay and pulse mode.

CD_BCK CD Bit Clock Input

The CD_BCK is the CD-Decoder bit clock. The SPCA718A can accept multiple BCK rates.

The CD-BCK can be set to multiple rates as in Table 5-1.

The CD input format can be selected by several programmable control bits. Six common CD data formats are presented in Table 5-2.

Table 5-1 BCK/Data rate/ LRCK relationships

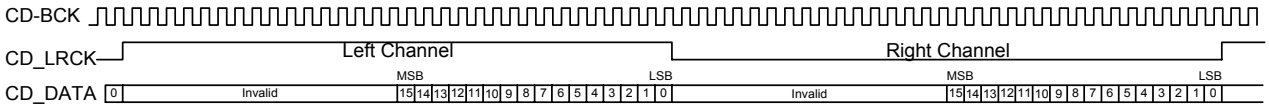
BCK	CD Speed	Data Rate	BCK Per LRCK
1.42 MHz	Normal	1.42 Mbits/sec	32
2.13 MHz	Normal	1.42 Mbits/sec	48
2.84 MHz	Normal	1.42 Mbits/sec	64
2.84 MHz	Double	2.84 Mbits/sec	32
4.26 MHz	Double	2.84 Mbits/sec	48
5.84 MHz	Double	2.84 Mbits/sec	64

Table 5-2 Common CDDSP configuration examples

Mode	BCK #	Data Endian	LRCK Left/Right Polarity	Data Latch Timing
1	32	MSB first	Right	1
2	32	MSB first	Left	0
3	24	MSB first	Right	1
4	24	LSB first	Right	0
5	24	MSB first	Right	1
6	16	MSB first	Left	1

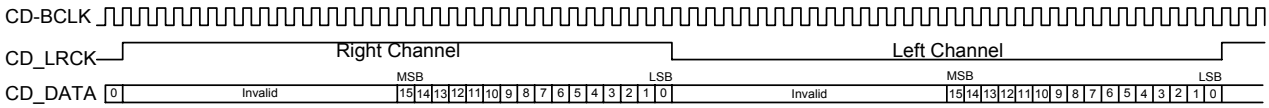
Functional timing diagrams of the above six formats are d etailed below:

CASE I (CD_CONFIG = 0x1012)



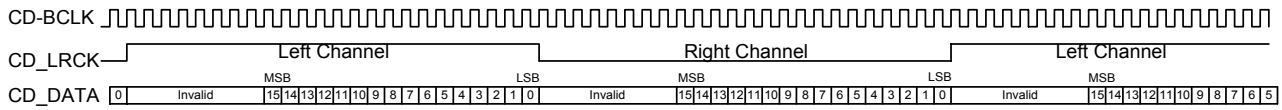
32-bit BCK, MSB First, Right Channel Low, Data latch timing high

CASE II (CD_CONFIG = 0x1003)



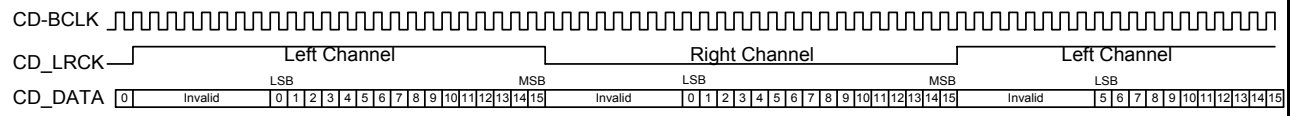
32-bit BCK, MSB First, Left Channel Low, Data latch timing low

CASE III (CD_CONFIG = 0x0812)



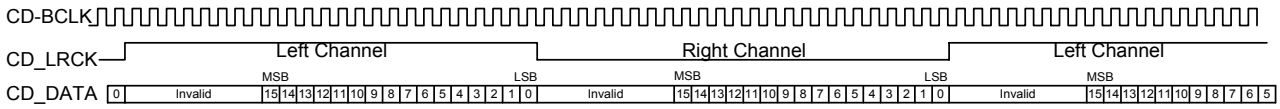
24-bit BCK, MSB First, Right Channel Low, Data latch timing low

CASE IV (CD_CONFIG = 0x0851)



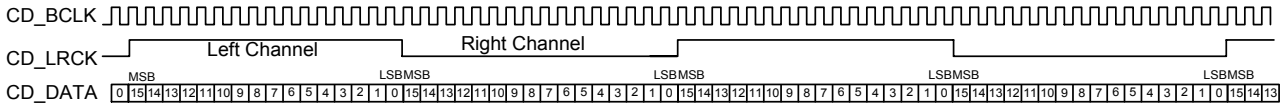
24-bit BCK, LSB First, Right Channel Low, Data latch timing low

CASE V (CD_CONFIG = 0x0813)



24-bit BCK, MSB First, Right Channel Low, Data latch timing high

CASE VI (CD_CONFIG = 0x0002)



16-bit BCK, MSB First, Left Channel Low, Data latch timing high

Figure 5-14 Timing diagrams of typical CD Input Formats in Table 5-2

Some common CD Sector Formats are presented below :

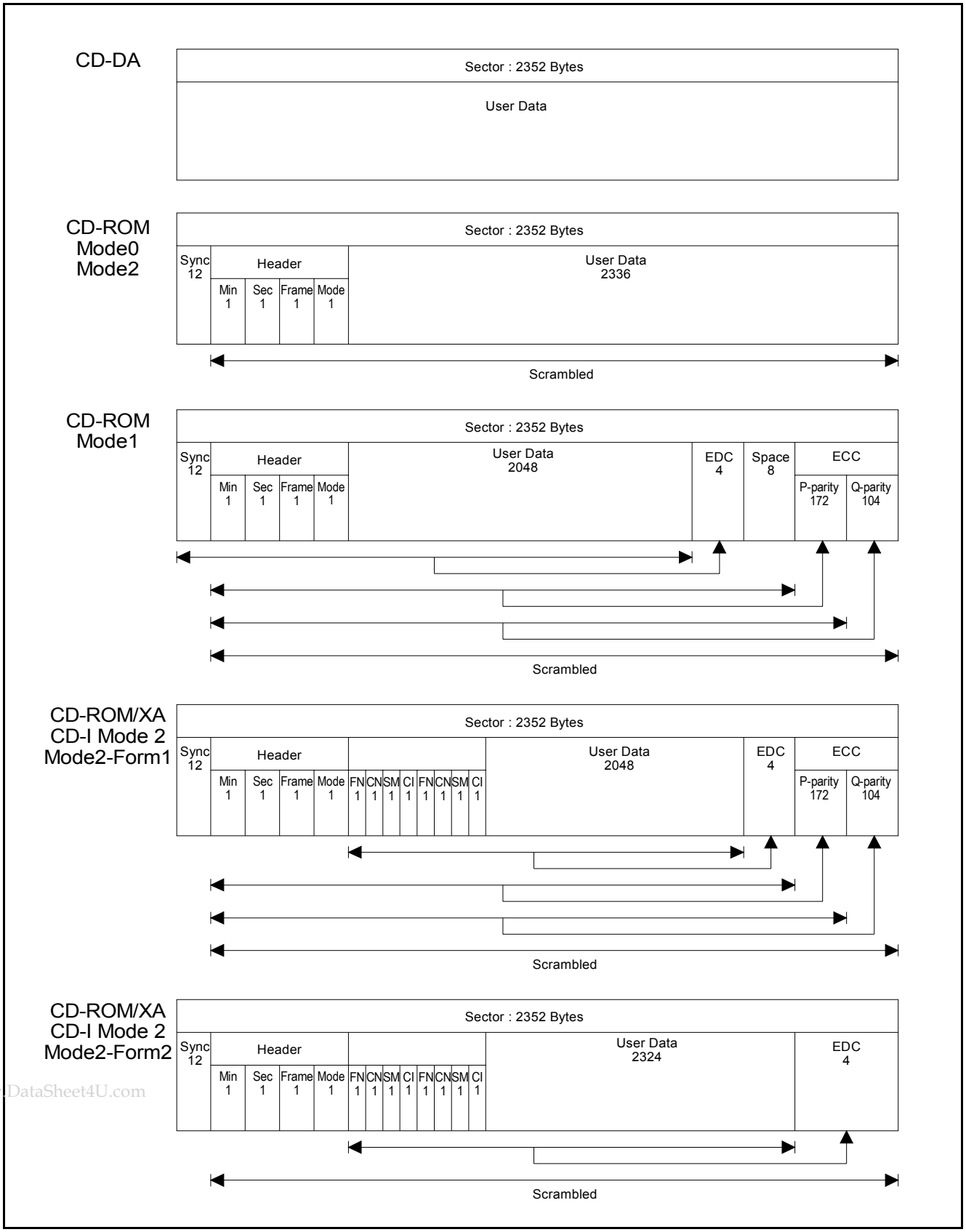


Figure 5-14 Some Common CD Sector Formats

5.10. Programmable I/O

The Programmable I/O (PIO) function as general-purpose I/O ports definable by the user. They can be used to gather external status information, drive internal status out, control external devices, communicate with external host or serve as interrupts for external host.

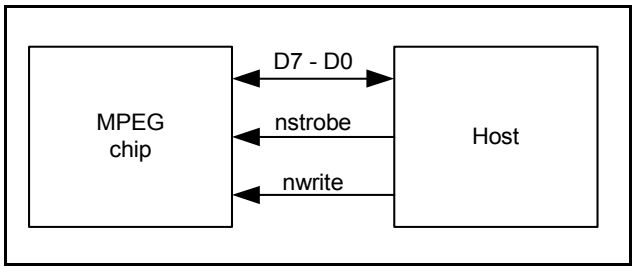
5.11. Host Interface

The SPCA718A provides flexible host interfaces to allow applications access to the SVCD or Audio/Video decoder functionality. These interfaces are as follows:

1.) UART

2.) Flexible GPIO control

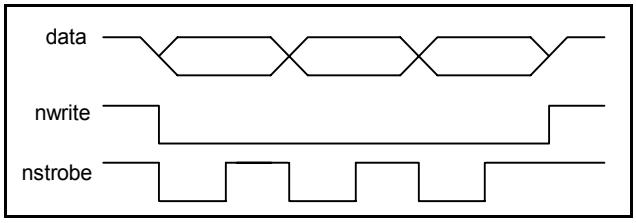
These host interface applications can co-work with SPCA718A A/V decoder and Parallel BUS. The host interface consist of ten signals which are D7 ~ D0, nstrobe and nwrite. The Mpeg chip is master and host is slave. Whenever the host want to access the MPEG, it has to read D0 ~ D7. At this time, the nstrobe and nwrite are high. The following table lists the defined actions that the host can take after reading.



Value Read	Host Action
00	host access is prohibited
01	host may read
02	host may write
03	host may read or write

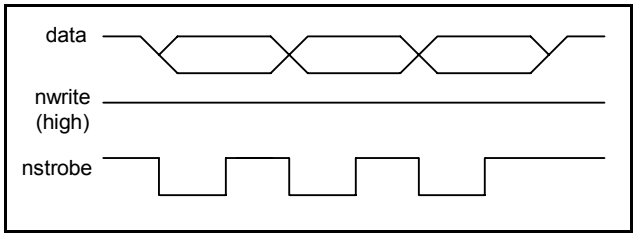
5.11.1. Host read timing

The following timing shows that the host writes three bytes into MPEG.



5.11.2. Host write timing

The following timing shows that the host reads three bytes from MPEG.



5.12. RISC Processor

The embedded 32-bit RISC processor helps to decode the high level data formats, MPEG system layers, low bandwidth MPEG audio and video decoding and assorted miscellaneous functions. If the SPCA718A were used in a low cost system with a simple user interface, additional savings could be accomplished by using the RISC core to perform host micro-controller functions. Thereby dropping the micro-controller from the bill-of-materials.

6.ELECTRICAL SPECIFICATIONS

6.1. Operating Conditions

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCCKP, VCCAP	Power Supply	-0.3 to 3.6	V
VCC5OP, VCC5IP, VCCTVP	Power Supply	-0.3 to 6	V
Tstg	Storage Temperature	-40 to 125	℃
Tsolder	Soldering Temp. (Max. Time)	240 (for 5 Sec. Max.)	℃

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VCCKP, VCCAP	Power Supply	3.0	3.3	3.6	V
VCC5OP, VCC5IP, VCCTVP	Power Supply	4.75	5.0	5.25	-
Vin	Input Voltage	0	-	5.0	V
Topr	Operating Temperature	0	-	70	℃

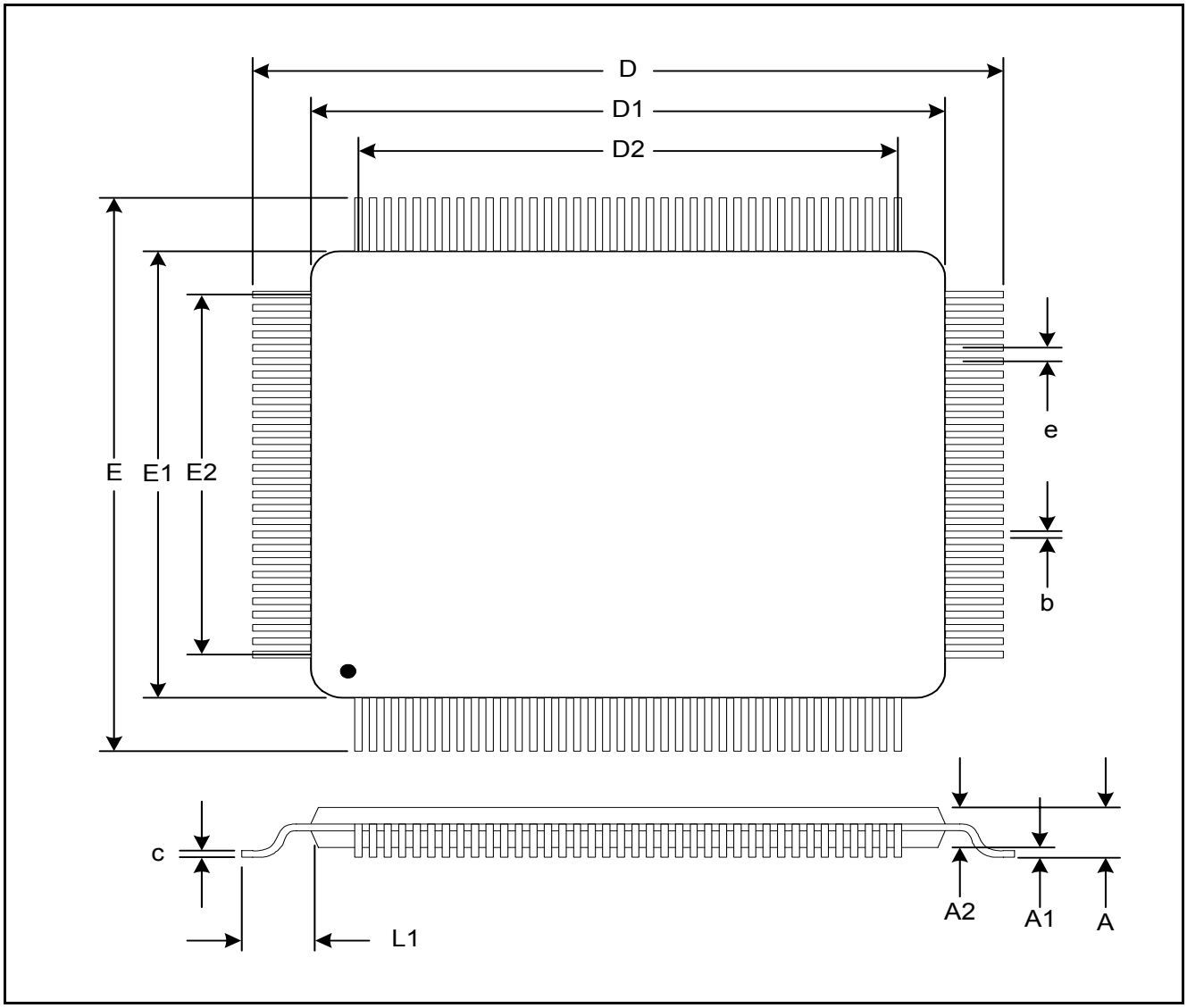
Table 6-3 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	-	-	0.8	V
V_{IH}	Input High Voltage	2.2	-	-	V
V_{OL}	Output Low Voltage	-	-	0.4	V
V_{OH}	Output High Voltage	4.75	5.0	5.25	V
I_{IL}	Input Low Current	-1.0	-	1.0	µA
I_{IH}	Input High Current	-1.0	-	1.0	µA
I_{OZ}	Tri-state leakage current	-1.0	-	1.0	µA
C_{IN}	Input Capacitance	-	2.8	-	pF
C_{OUT}	Output Capacitance	2.7	-	5.6	pF
C_{BID}	Bidirectional Capacitance	2.7	-	5.6	pF

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.PACKAGE/PAD LOCATIONS

7.1. Package Outline Dimensions



Symbol	Min.	Nom.	Max.	Unit
D	-	22	-	Millimeter
D1	-	20	-	Millimeter
D2	-	18.5	-	Millimeter
E	-	16	-	Millimeter
E1	-	14	-	Millimeter
E2	-	12.5	-	Millimeter
e	-	0.5	-	Millimeter
b	0.17	0.20	0.27	Millimeter
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
c	0.09	-	0.20	Millimeter
L1	-	1.6	-	Millimeter

8.DISCLAIMER

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9.REVISION HISTORY

Date	Revision #	Description	Page
MAR. 11, 2002	0.1	Original	25