

FDFS2P102

Integrated P-Channel MOSFET and Schottky Diode

General Description

The FDFS2P102 combines the exceptional performance of Fairchild's high cell density MOSFET with a very low forward voltage drop Schottky barrier rectifier in an SO-8 package.

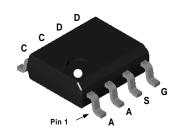
This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance. The independently connected Schottky diode allows its use in a variety of DC/DC converter topologies.

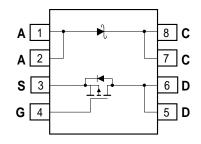
Applications

- DC/DC converters
- Load Switch
- Motor Drives

Features

- -3.3 A, -20 V. $R_{DS(ON)} = 0.125~\Omega$ @ $V_{GS} = -10~V$ $R_{DS(ON)} = 0.200~\Omega$ @ $V_{GS} = -4.5~V$.
- $V_F < 0.39 V @ 1 A (T_J = 125 {}^{o}C)$. $V_F < 0.47 V @ 1 A$. $V_F < 0.58 V @ 2 A$.
- Schottky and MOSFET incorporated into single power surface mount SO-8 package.
- Electrically independent Schottky and MOSFET pinout for design flexibility.





MOSFET Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Drain Current - Continuous	(Note 1a)	-3.3	Α
	- Pulsed		-20	
P _D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C

Schottky Diode Maximum Ratings TA=25°C unless otherwise noted

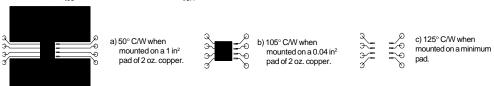
V_{RRM}	Repetitive Peak Reverse Voltage		20	V
Io	Average Forward Current	(Note 1a)	1	Α

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDFS2P102 FDFS2P102 13		12mm	2500 units	

Symbol	Parameter	Test C	onditions	Min	Тур	Max	Units
Off Char	acteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D$	= -250 µA	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V},$	*			-1	μΑ
	•	$V_{GS} = 0 V$	$T_J = 55^{\circ}C$			-10	
I _{GSSF}	Gate-Body Forward Leakage	$V_{GS} = 20 \text{ V}, \text{ V}$	$V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate-Body Reverse Leakage	$V_{GS} = -20 \text{ V},$	$V_{DS} = 0 V$			-100	nA
On Char	acteristics (Note 2)	•		-	,		,
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D}$	= -250 µA	-1	-1.4	-2	V
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V},$			0.100	0.125	Ω
**DS(0II)	Statio Brain Course on Recicianes	$V_{GS} = -4.5 \text{ V},$			0.167	0.2	1
I _{D(on)}	On-State Drain Current	$V_{GS} = -10 \text{ V}, \text{ V}$		-10			Α
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I			5		S
	Characteristics				!	!	
C _{iss}	Characteristics Input Capacitance	V _{DS} = -10 V, Y	$V_{GS} = 0 \text{ V}.$		270		pF
Coss	Output Capacitance	f = 1.0 MHz	- 7		150		pF
C _{rss}	Reverse Transfer Capacitance	İ		45		pF	
Switchin t _{d(on)}	g Characteristics (Note 2) Turn-On Delay Time	V _{DD} = -15 V,	I _D = -1 A,		8	16	ns
tr	Turn-On Rise Time	V_{GS} = -10 V, R_{GEN} = 6 Ω			7	14	ns
t _{d(off)}	Turn-Off Delay Time				17	27	ns
t _f	Turn-Off Fall Time	$V_{DS} = -5 \text{ V}, I_D = -3.3 \text{ A}, V_{GS} = -10 \text{ V},$			10	1.8	ns
Q _g	Total Gate Charge				7	10	nC
Drain-Sc	ource Diode Characteristics ar	nd Maximur	n Ratings				
Is	Maximum Continuous Drain-Source Di	ode Forward C	Current			-1.3	Α
V_{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -1.3 A (Note 2)			-0.8	-1.2	V
Schottky	/ Diode Characteristics						
l _R	Reverse Leakage	V _R = 20 V	$T_J = 25^{\circ}C$			250	uA
-10		1, 2,	$T_{\rm J} = 125^{\circ}{\rm C}$			18	mA
V _F	Forward Voltage	I _F = 1 A	$T_J = 25^{\circ}C$			0.47	V
			T _J = 125°C			0.39	
		$I_F = 2 A$	$T_1 = 25^{\circ}C$			0.58	
			$T_{\rm J} = 125^{\circ}{\rm C}$			0.53	
<u>Thermal</u>	Characteristics			1			·
R JA	Thermal Resistance, Junction-to-Ambient (Note 1a)				78		
R _{JC}	Thermal Resistance, Junction-to-Case (Note 1)				40		

^{1:} $R_{\theta IA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



Scale 1 : 1 on letter size paper

^{2:} Pulse Test: Pulse Width $\leq\!300\,\mu\text{s}$, Duty Cycle $\leq\!2.0\%$

Typical Characteristics

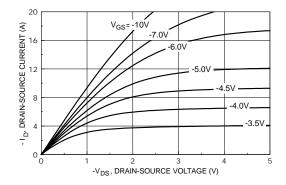


Figure 1. On-Region Characteristics.

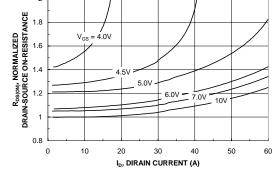


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

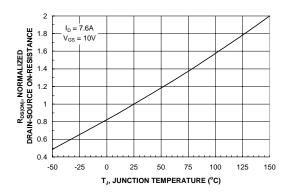


Figure 3. On-Resistance Variation with Temperature.

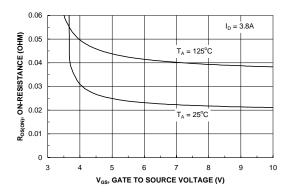


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

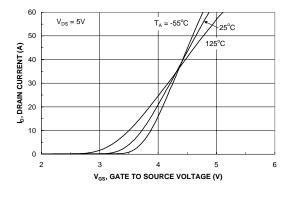


Figure 5. Transfer Characteristics.

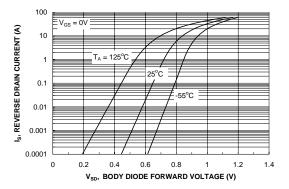
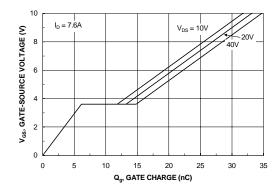


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)



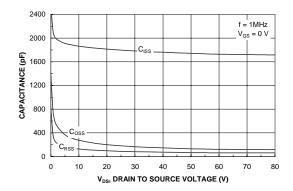
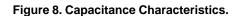
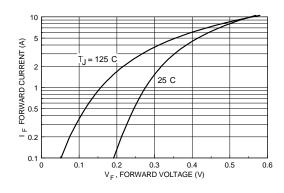


Figure 7. Gate-Charge Characteristics.





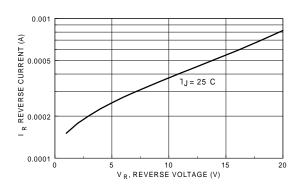


Figure 9. Schottky Diode Forward Voltage.

Figure 10. Schottky Diode Reverse Current.

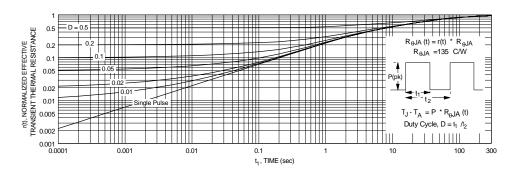


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient themal response will change depending on the circuit board design.

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