FA5510P (N), FA5511P (N)
FA5514P (N), FA5515P (N)

■ Description

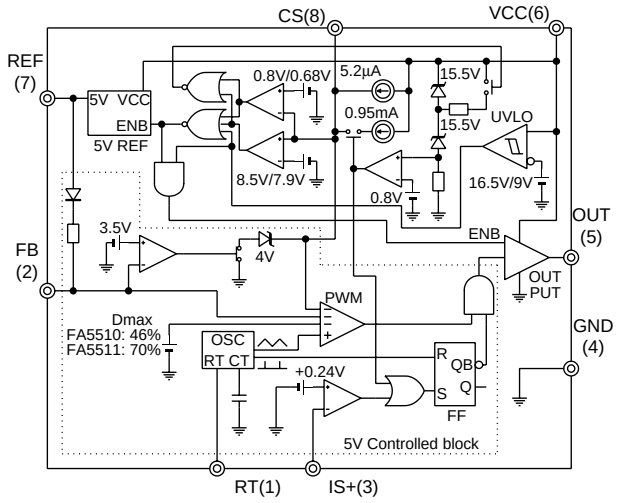
The FA551X series are the PWM type switching power supply control ICs that can directly drive power MOSFET. These ICs use a CMOS device with high dielectric strength (30V) to implement low power consumption. These ICs contain many function in a small 8-pin package. With these ICs, a high-performance and compact power supply can be created because not many external discrete components are needed.

■ Features

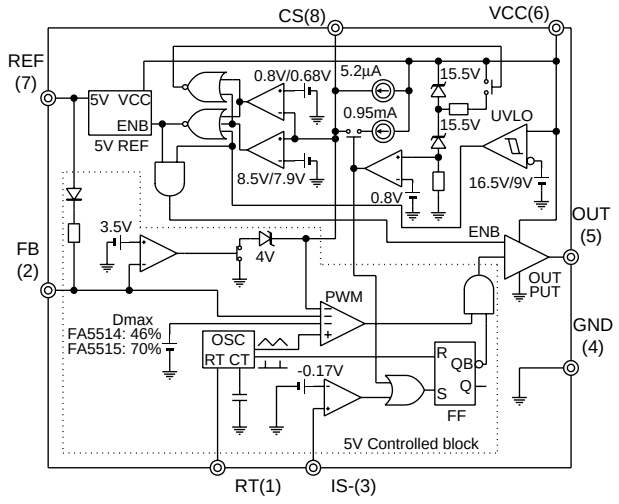
- Low current consumption by CMOS process with high dielectric strength (30V)
- Standby current of 2μA or less (at Vcc=14V), and operating current of 1.5mA (typ)
- Overvoltage protection function detecting the Vcc voltage
- A drive circuit for connecting a power MOSFET directly
- Output peak current: ±1.5A
- Pulse-by-pulse overcurrent limiting function
- Overload protection function (latch or non-latch mode selectable)
- Output ON-OFF function by external signal
- Latch-mode overvoltage shutdown function
- Undervoltage lockout function (16.5V ON / 9V OFF)
- Reference voltage output (5V)
- 8-pin package (DIP/SOP)

■ Block diagram

● **FA5510P (N), FA5511P (N)**

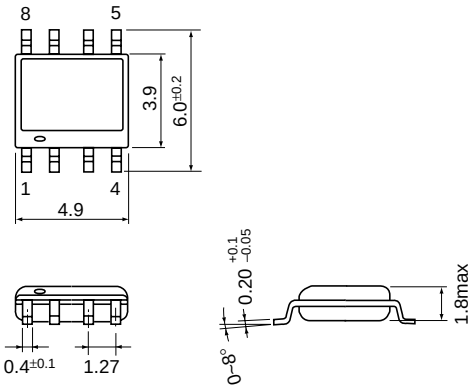


● **FA5514P (N), FA5515P (N)**

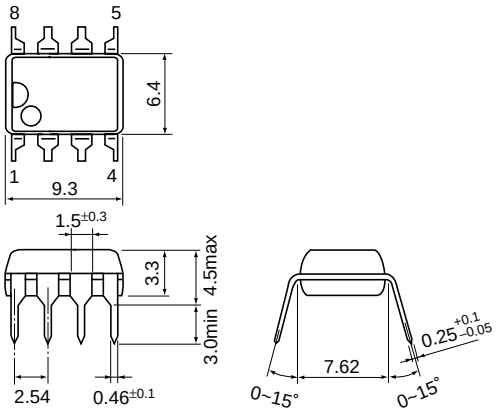


■ Dimensions, mm

● **SOP-8**



● **DIP-8**



Pin No.	Pin symbol	Function	Description
1	RT	Oscillator timing resistor	Setting oscillation frequency
2	FB	Feedback	Input of PWM comparator
3	IS	Overcurrent detection	Input of the overcurrent limiting function
4	GND	Ground	Ground
5	OUT	Output	Output for driving a power MOSFET
6	VCC	Power supply	Power supply
7	REF	Reference voltage	Reference voltage output (5V)
8	CS	Soft-start and ON/OFF control	Soft-start, ON/OFF function and latch-mode shutdown operations

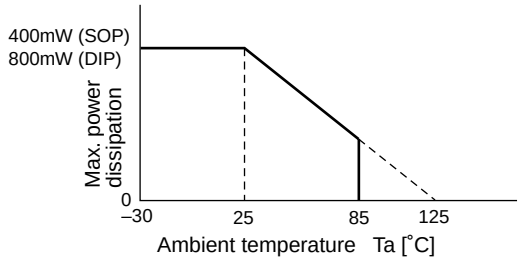
Type	Max. duty cycle (typ.)	Polarity of overcurrent detection	Package
FA5510P	46%	+	DIP-8
FA5510N			SOP-8
FA5511P	70%	+	DIP-8
FA5511N			SOP-8
FA5514P	46%	–	DIP-8
FA5514N			SOP-8
FA5515P	70%	–	DIP-8
FA5515N			SOP-8

■ Absolute maximum ratings

Item		Symbol	Rating	Unit
Supply Voltage	Low impedance source (I_{CC}>15mA)	V_{CC1}	30	V
	Internal zener clamp (I_{CC}<15mA)	V_{CC2}	Self limiting	V
Output peak current		I_{OUT}	±1.5	A
FB pin input voltage		V_{FB}	–0.3 to 5.0	V
IS pin input voltage		V_{IS}	–0.3 to 5.0	V
REF pin source current		I_{REF}	–10	mA
CS pin sink current		I_{CS}	+2.0	mA
Total power dissipation (Ta=25˚C)		Pd	800 (DIP-8) 400 (SOP-8)	mW
Ambient temperature		Ta	–30 to +85	˚C
Maximum junction temperature		Tj	125	˚C
Storage temperature		Tstg	–40 to +150	˚C

Note: There are cases where the IC cannot output the rating current depending on Vcc voltage or temperature.

Maximum power dissipation curve



■ Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	10		28	V
Oscillation frequency	f_{OSC}	10		500	kHz
REF-GND capacitor	Cref	0.1	0.47		µF
Soft start capacitor	C_S	0.01		1	µF

■ Electrical characteristics (V_{CC}=18V, R_T=47kΩ, Ta=25˚C)

Reference voltage section (REF pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Reference voltage	V_{REF}	Tj=25˚C	4.75	5.00	5.25	V
Line regulation	V_{dv1}	V_{CC}=10 to 28V		±6	±20	mV
Load regulation	V_{dv2}	I_L=0 to 10mA, V_{CC}=18V	–40	–12		mV
Temperature stability	V_{dT}	Ta=–30 to 85˚C		±0.5		mV/˚C

Oscillator section (RT pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	R_T=47kΩ, Tj=25˚C	92.6	100	107.4	kHz
Voltage stability	f_{dv}	V_{CC}=10 to 28V		±1.0		%
Temperature stability	f_{dT}	Ta=–30 to 85˚C		±0.02		%/˚C

Pulse width modulation circuit section (FB pin)

Item	Symbol	Test condition	FA5510/14			FA5511/15			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
FB pin source current	I_{FB}	V_{FB}=0	–855	–720	–585	–855	–720	–585	µA
Input threshold voltage (FB pin)	$V_{TH\ FB0}$	Duty cycle =0%	0.9	1		0.9	1		V
	$V_{TH\ FBM}$	Duty cycle =D_{MAX}		1.92			2.40		V
Maximum duty cycle	D_{MAX}		42	46	50	66	70	74	%

Overcurrent limiting circuit section (IS pin)

Item	Symbol	Test condition	FA5510/11			FA5514/15			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input threshold voltage (IS pin)	V_{THIS}		220	240	260	–190	–170	–150	mV
Source current (IS pin)	I_{IS}	V_{IS}=0V			±5	–28	–20	–12	µA
Delay time	t_{pdIS}			150			150		ns

Soft start circuit section (CS pin)

Item	Symbol	Test condition	FA5310/14			FA5311/15			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Charge current (CS pin)	I_{CHG}	V_{CS}=1V, Tj=25˚C	–7.2	–5.2	–3.2	–7.2	–5.2	–3.2	µA
Input threshold voltage (CS pin)	$V_{TH\ CS0}$	Duty cycle =0%	0.90	1.0		0.90	1.0		V
	$V_{TH\ CSM}$	Duty cycle =D_{MAX}		1.92			2.40		V

Output ON/OFF control circuit section (CS pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Source current (CS pin)	I_{S0CS}	V_{CS}=0V, Tj=25˚C	–7.2	–5.2	–3.2	µA
ON/OFF control threshold voltage (CS pin)	V_{THON}	OFF→ON, Tj=25˚C		0.8	0.93	V
	V_{THOFF}	ON→OFF, Tj=25C	0.50	0.68		V
Hysteresis voltage	V_{THOHS}			0.12		V

Latch-mode cutoff circuit section (CS pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Sink current (CS pin)	I_{SICS}	V_{CS}=6.5V, V_{FB}=1V, Tj=25˚C	18	30	45	µA
Cutoff threshold voltage (CS pin)	$V_{TH\ CSF}$	ON→OFF, Tj=25˚C	8.0	8.5	9.0	V
	$V_{TH\ CSN}$	OFF→ON, Tj=25˚C	7.4	7.9	8.4	V
Hysteresis voltage	V_{THHIS}			0.6		V

Overload cutoff circuit section (FB pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Overload threshold voltage (FB pin)	$V_{TH\ FB}$		3.2	3.5	3.8	V

Overvoltage cutoff circuit section (VCC pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Overvoltage threshold voltage (VCC pin)	$V_{TH\ VCC}$	Tj=25˚C	30	31.8	34	V
Cutoff operating supply current (VCC pin)	I_{VCC}	Tj=25˚C, V_{CC}=V_{THVCC}		14		mA
Charge current (CS pin)	I_{S0CS2}	V_{CS}=6.5V	–1.4	–0.95	–0.5	mA

Undervoltage lockout circuit section (VCC pin)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
OFF-to-ON threshold voltage	$V_{CC\ ON}$	Tj=25˚C	15.5	16.5	17.5	V
ON-to-OFF threshold voltage	$V_{CC\ OFF}$	Tj=25˚C	8.5	9.0	10.0	V
Hysteresis voltage	V_{HYS}	Tj=25˚C	6.8	7.5	8.2	V

Output circuit section (OUT pin)

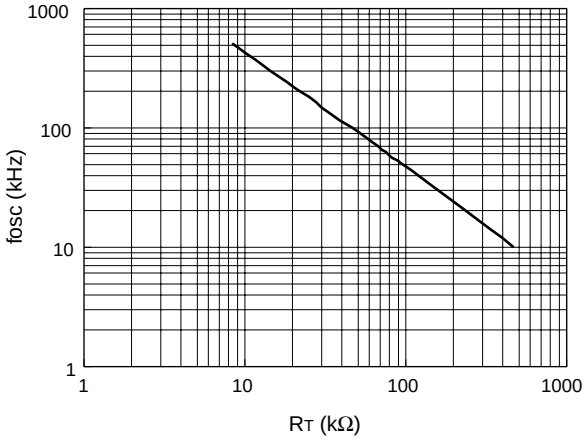
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Low output voltage	V_{OL}	I_{OL}=100mA		0.7	1.5	V
High output voltage	V_{OH}	I_{OH}=–100mA, V_{CC}=18V	15	16.5		V
Rise time	tr	C_L=1nF		40		ns
Fall time	tf	C_L=1nF		25		ns

Supply current (VCC pin)

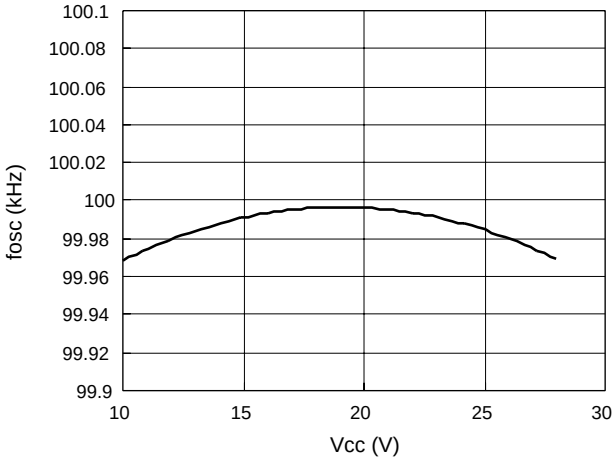
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Stand-by current	I_{CCSTB}	V_{CC}=14V			2	µA
Startup current	I_{CCST}	V_{CC}=OFF-to-ON threshold voltage		12	30	µA
Operating-state supply current	I_{CCOP}	No load		1.5	2.5	mA
OFF-state supply current	I_{CCOF}	V_{CC}=17V, CS=0V		80	200	µA
Latch mode supply current	I_{CCL}	V_{CC}=10V		45	80	µA

■ Characteristic curves (V_{CC}=18V, R_T=47kΩ, Ta=25˚C)

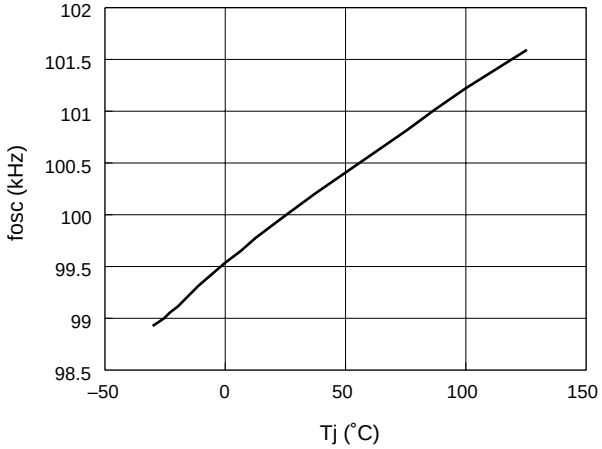
Oscillation frequency (f_{OSC}) vs. timing resistor resistance (R_T)



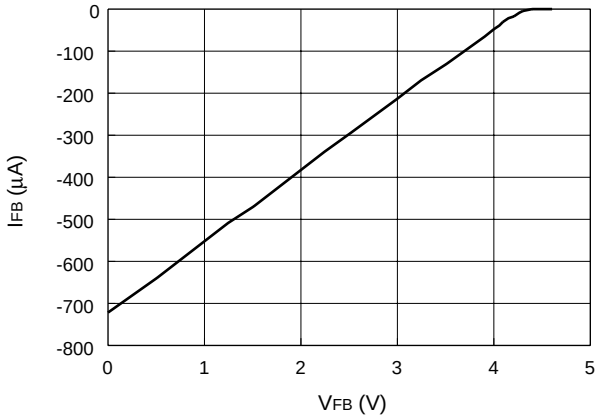
Oscillation frequency (f_{OSC}) vs. supply voltage (V_{CC})



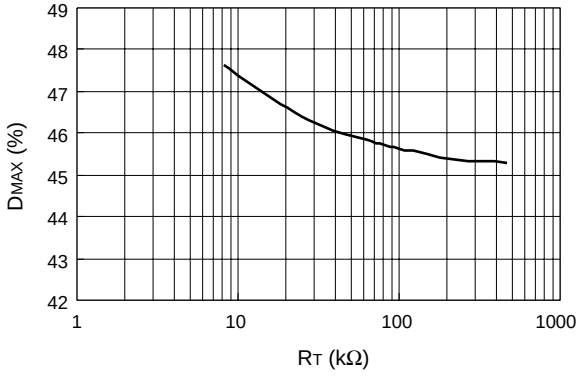
Oscillation frequency (f_{OSC}) vs. junction temperature (Tj)



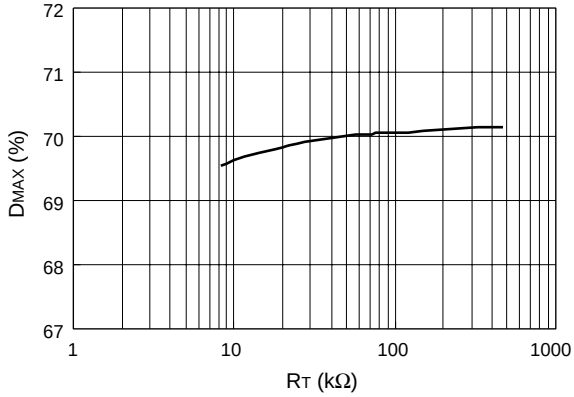
FB pin source current (I_{FB}) vs. FB pin voltage (V_{FB})



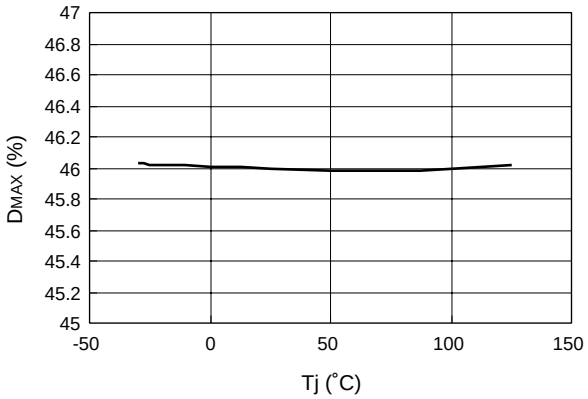
Maximum duty cycle (D_{MAX}) vs. timing resitor resistance (R_T)
FA5510/14



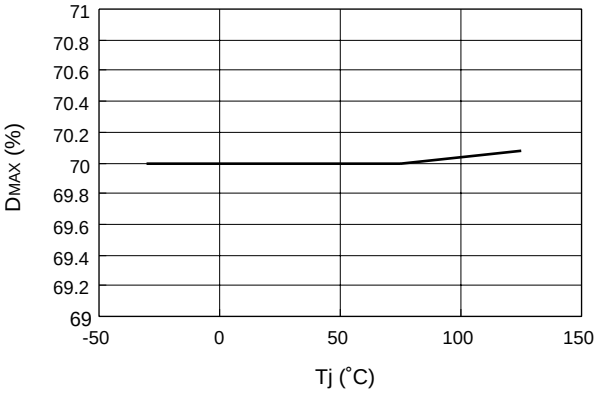
Maximum duty cycle (D_{MAX}) vs. timing resitor resistance (R_T)
FA5511/15



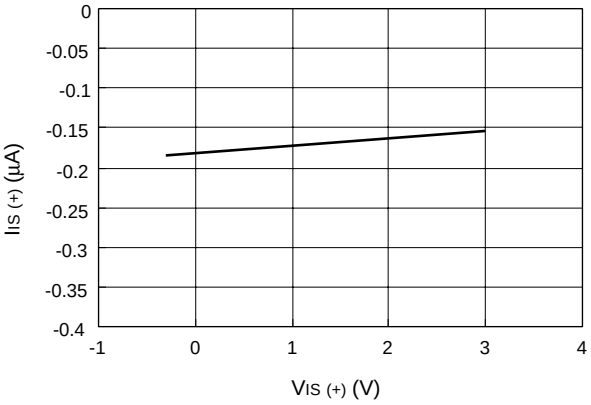
Maximum duty cycle (D_{MAX}) vs. junction temperature (Tj)
FA5510/14



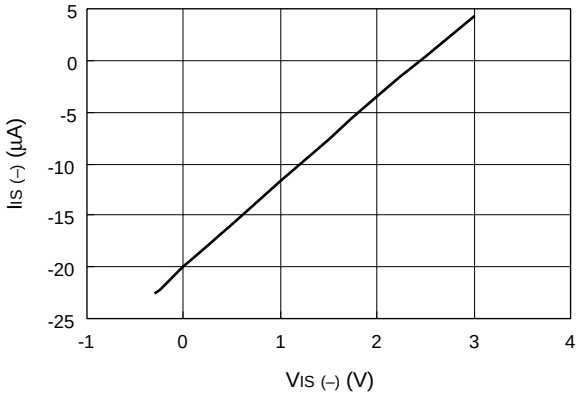
Maximum duty cycle (D_{MAX}) vs. junction temperature (Tj)
FA5511/15



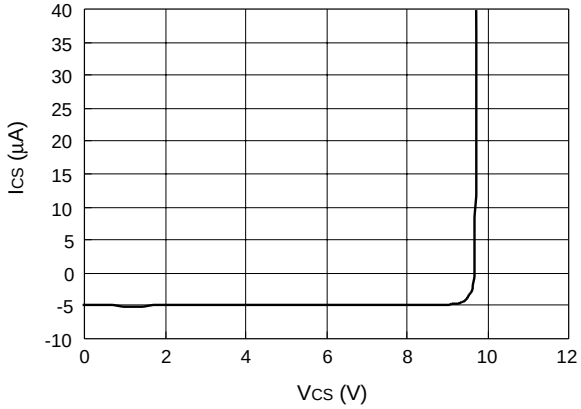
IS (+) pin current ($I_{IS(+)}$) vs. IS (+) pin voltage ($V_{IS(+)}$)
FA5510/11



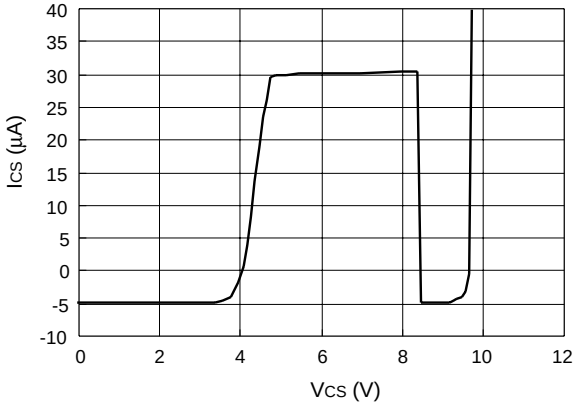
IS (–) pin current ($I_{IS(-)}$) vs. IS (–) pin voltage ($V_{IS(-)}$)
FA5514/15



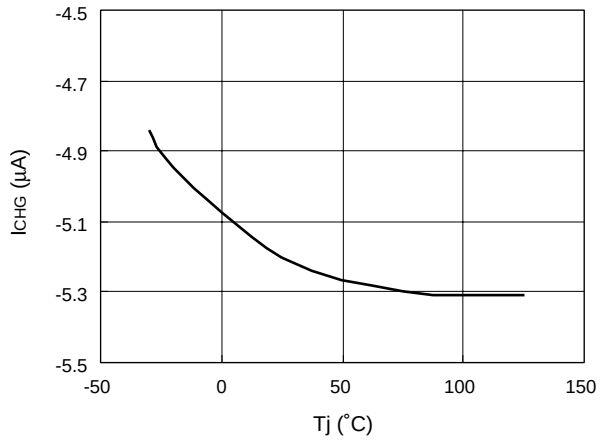
CS pin current (I_{CS}) vs. CS pin voltage (V_{CS})
FB=open



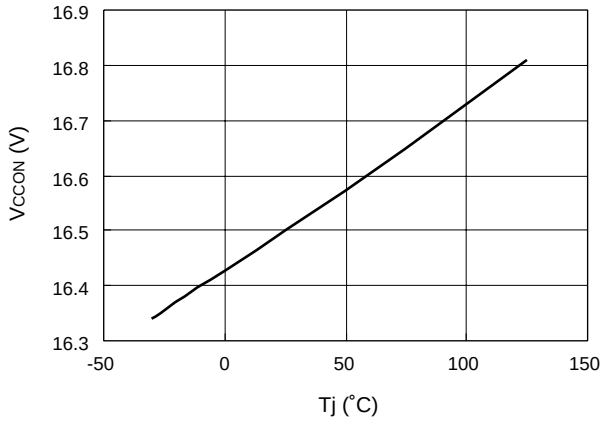
CS pin current (I_{CS}) vs. CS pin voltage (V_{CS})
FB=0V



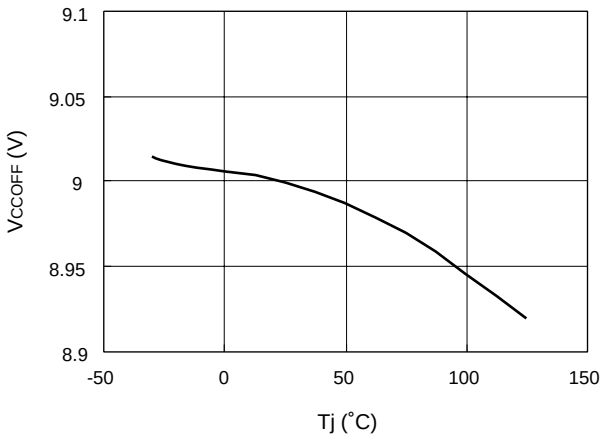
CS pin charge current (I_{CHG}) vs. junction temperature (Tj)



UVLO OFF-to-ON threshold voltage (V_{CCON}) vs. junction temperature (Tj)

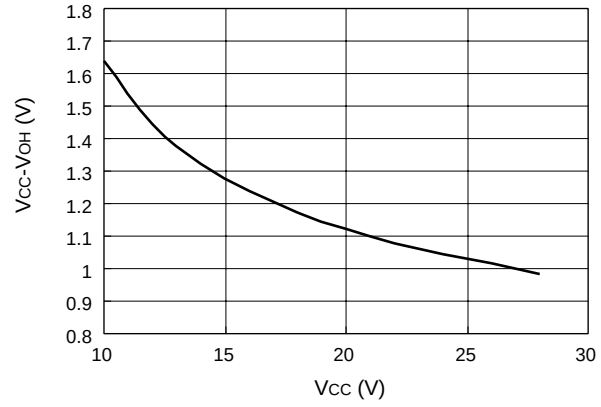


UVLO ON-to-OFF threshold voltage (V_{CCOFF}) vs. junction temperature (Tj)



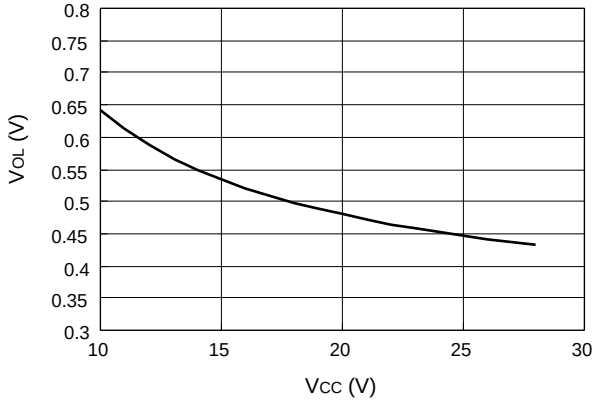
H-level output voltage (V_{OH}) vs. supply voltage (V_{CC})

I_O= –100mA

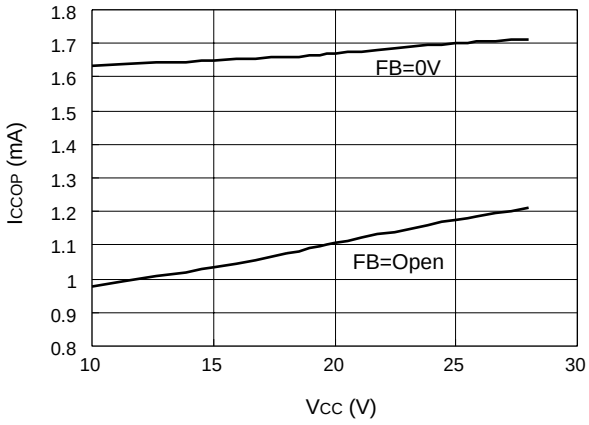


L-level output voltage (V_{OL}) vs. supply voltage (V_{CC})

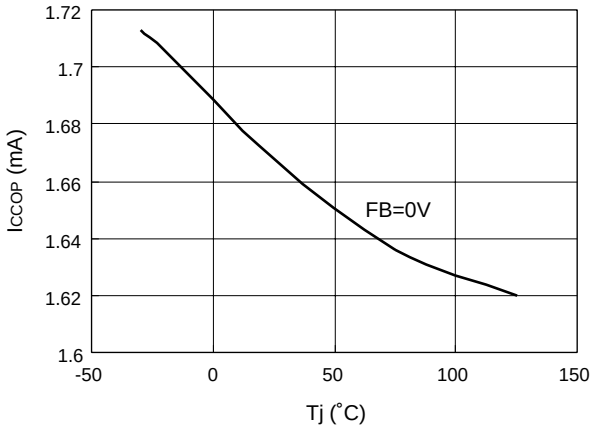
I_O=100mA



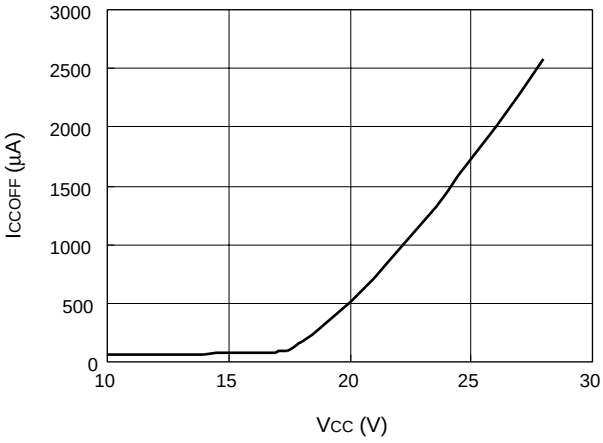
Operating state supply current (I_{CCOP}) vs. supply voltage (V_{CC})



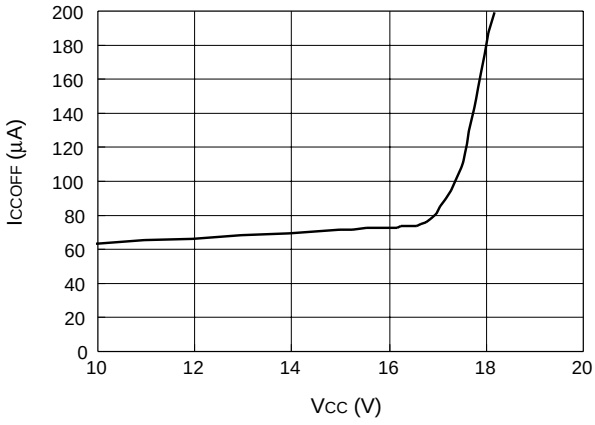
Operating state supply current (I_{CCOP}) vs. junction temperature (Tj)



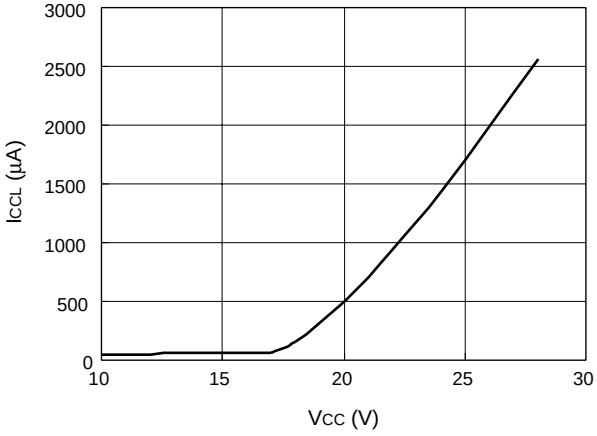
OFF state supply current (I_{CCOFF}) vs. supply voltage (V_{CC})



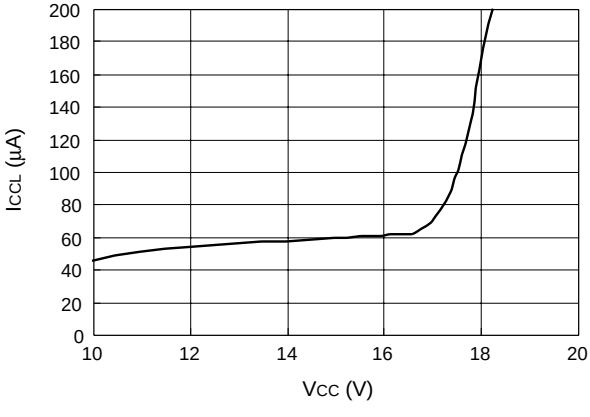
OFF state supply current (I_{CCOFF}) vs. supply voltage (V_{CC})
Enlarged



Latch mode supply current (I_{CCL}) vs. supply voltage (V_{CC})



Latch mode supply current (I_{CCL}) vs. supply voltage (V_{CC})
Enlarged



■ Description of each circuit

1. Oscillator

The oscillator generates a triangular waveform by charging and discharging the built-in capacitor. A desired oscillation frequency can be set by the value of the resistor connected to the RT pin (See Figure 1).

The built-in capacitor voltage oscillates between about 3V and 1V, with almost the same charging and discharging gradients (Figure 2). You can set the desired oscillation frequency by changing the gradients using the resistor connected to the RT pin. (Large R_T=Low frequency, small R_T=High frequency)
The relationship between R_T and the oscillation frequency is approximately given by:

$$f_{OSC} \fallingdotseq \frac{4880}{R_T + 1.4}\ [kHz] \quad \cdots\cdots (1)$$

$$R_T \fallingdotseq \frac{4880}{f_{OSC}} - 1.4\ [k\Omega] \quad \cdots\cdots (2)$$

f_{OSC}: Oscillation frequency [kHz]
R_T: Timing resistance [kΩ]

The oscillator waveform cannot be observed from the outside because the oscillator output is not pinned out. The oscillator output is connected to a PWM comparator.

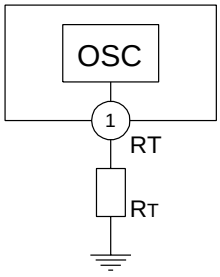


Fig. 1 Oscillator

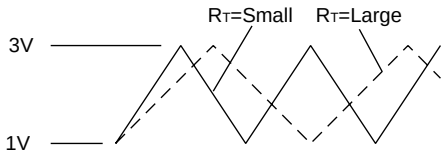


Fig. 2 Oscillator output

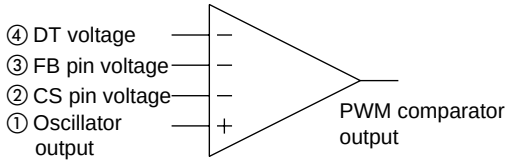


Fig. 3 PWM comparator

2. PWM comparator

The PWM comparator has four inputs as shown in Figure 3. Oscillator output ① is compared with CS pin voltage ②, FB pin voltage ③, and DT voltage ④. The lowest of three inputs ②, ③, and ④ has priority and is compared with oscillator output ①. While the voltage is lower than the oscillator output, the comparator output is high. While the voltage is higher than the oscillator output, the PWM comparator output is low (see Figure 4). The IC OUT pin voltage is high while the PWM comparator output is low. When the IC is powered up, CS pin voltage ② controls soft start operation. The output pulse then begins to widen gradually. During normal operation, the output pulse width is determined within the maximum duty cycle (FA5510/14: 46%, FA5511/15: 70%) set by DT voltage ④ under the condition set by FB pin voltage ②, to stabilize the output voltage.

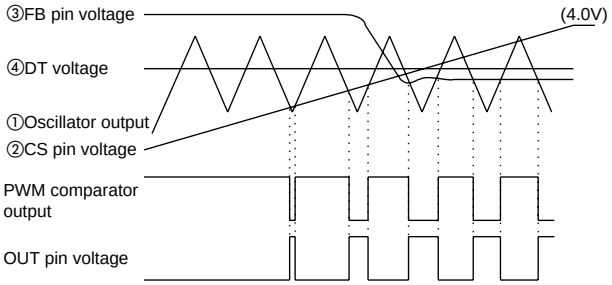


Fig. 4 PWM comparator timing chart

3. CS pin circuit

As shown in Figure 5, capacitor Cs is connected to the CS pin. The CS pin voltage varies depending on the charging voltage of this capacitor Cs.
When the power is turned on, the constant current source (5.2µA) begins to charge capacitor. Accordingly, the CS pin voltage rises as shown in Figure 6. The CS pin voltage is connected to the PWM comparator, which is characterized to make output based on the lowest of input voltages. The device enters soft-start mode while the CS pin voltage is between 1.0V and V_{THCSM} (FA5510/14: 1.92V, FA5511/15: 2.4V).
During normal operation, the CS pin is clamped at 4.0V by internal zener diode. If the output voltage drops due to an overload and the FB voltage rises to 3.5V or more, the clamp voltage 4.0V is canceled and the CS pin voltage rises to 9.5V. The CS pin is also connected to latch comparator C2. If the CS pin voltage rises to 8.5V or more, comparator C2 toggles to turn off the 5V REF circuit, thereby shutting the output down.
Since the CS pin is also connected to comparator C1, the 5V REF circuit can be turned off to shut the output down by dropping the CS pin voltage below 0.68V. In this way, comparator C1 can be used for output on-off control.
As explained above, the CS pin can be used for soft-start, overload output shutdown, and output on-off control by varying the voltage. Further details on the above three major functions of the CS pin are given below.

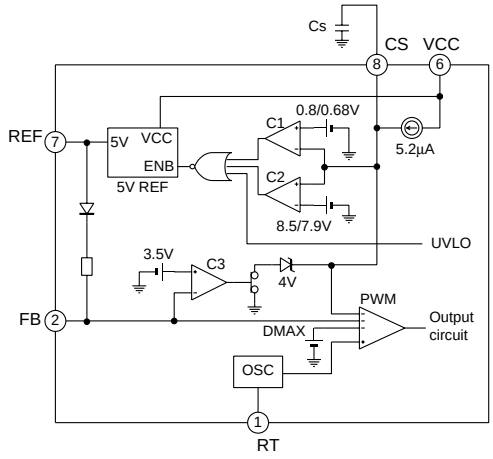


Fig. 5 CS pin circuit

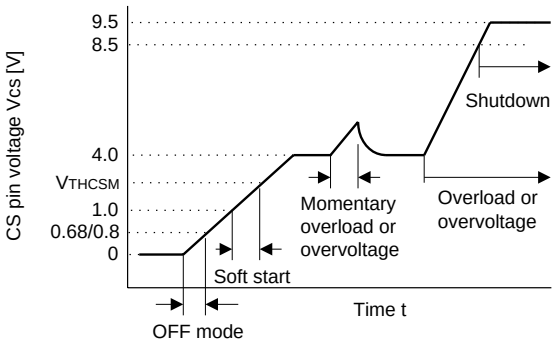


Fig. 6 CS pin waveform

3.1 Soft start function

Figure 7 shows the soft start circuit. Figure 8 is a soft-start operation timing chart. The CS pin is connected to capacitor Cs. When the power is turned on, the constant current source (5.2µA) begins to charge the capacitor. As shown in the timing chart, the CS pin voltage rises slowly in accordance with the capacitor Cs charging current. The CS pin is also connected to the IC internal PWM comparator, which has such characteristics that the voltage is determined to output on the basis of the lowest of input voltages. The comparator output pulse slowly widens to cause a soft start as shown in the timing chart.
The soft start period can be approximately estimated by the period ts, from the time the IC is activated to the time the output pulse width widens to 30%. The period ts is given by the following equation:

$$t_S\ [ms] \fallingdotseq 310 \times C_S\ [ms] \quad \cdots\cdots (3)$$

Cs: Soft start capacitor [µF]

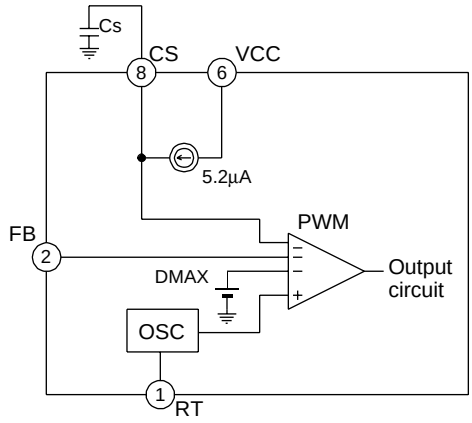


Fig. 7 Soft start circuit

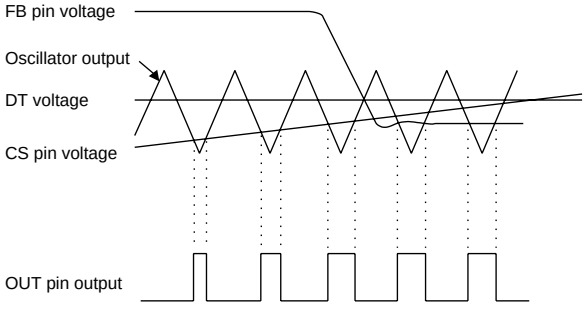


Fig. 8 Soft start timing chart

3.2 Overload shutdown function

Figure 9 shows the overload shutdown circuit, and Figure 10 is a timing chart that illustrates overload shutdown operation.
If the output voltage drops due to an overload or short circuit, the FB pin output voltage rises. If the FB pin voltage exceeds the reference voltage (3.5V) of comparator C3, the output of comparator C3 goes low to turn off the switch. With the switch off, the CS pin voltage clamped at 4.0V by zener diode in normal operation is unclamped, and the constant current source (5.2µA) begins to charge capacitor Cs again and the CS pin voltage rises. When the CS pin voltage exceeds the reference voltage (8.5V) of comparator C2, the output of comparator C2 toggles to turn off the 5V REF circuit. The IC then enters the latched mode and shuts down the output. IC current consumption for shutdown is 45µA (typ) (Vcc=10V). This current must be supplied through the startup resistor. The IC enters output off (low voltage) state.
The overload shutdown operation can be reset by lowering the supply voltage Vcc to below the OFF threshold voltage (9.0V) or forcing the CS pin voltage below 7.9V.
The period t_{OL} from the time the output is short-circuited to the time the output circuit goes off is given by the following equation:

$$t_{OL}\ [ms] \fallingdotseq 870 \times C_S\ [ms] \quad \cdots\cdots (4)$$

C_S: Soft start capacitor [µF]

When you want to disable the overload shutdown function, see item 9 in “Design advice”

3.3 Output ON/OFF control function

The IC can be turned on or off via an external signal applied to the CS pin. Figure 11 shows the output on/off control circuit, and Figure 12 is a timing chart. The IC is turned off when the CS pin voltage is externally made to drop below 0.68V (typ). The output of comparator C1 goes high to turn the 5V REF circuit off. This shuts the output down. The IC enters output off (low voltage) state. Required IC current consumption during shutdown is 80µA (typ) (Vcc=17V). This current must be supplied through the startup resistor. The IC goes on when the CS pin is opened and the CS pin voltage exceeds 0.80V (typ). This turns the 5V REF circuit on and results in automatic soft start. The power supply then restarts operation.

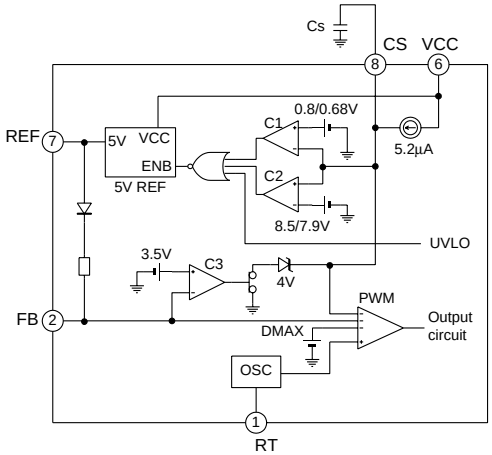


Fig. 9 Overload shutdown circuit

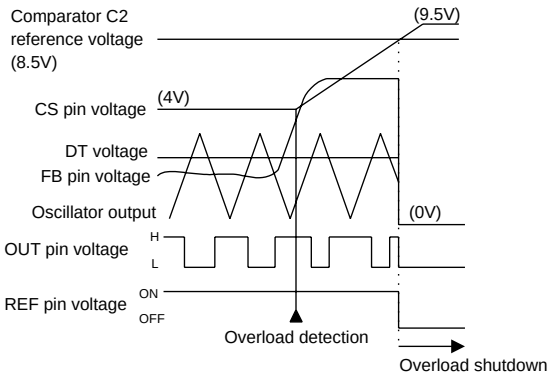


Fig. 10 Overload shutdown timing chart

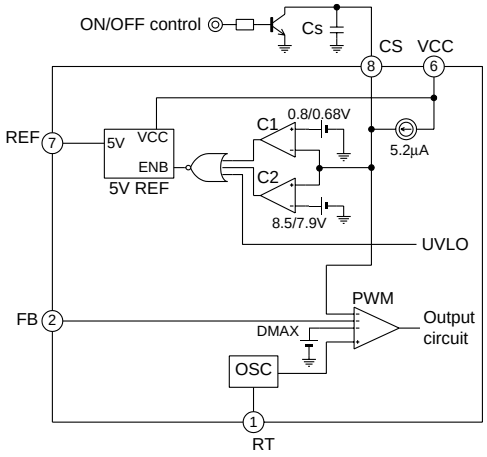


Fig. 11 External output ON/OFF control circuit

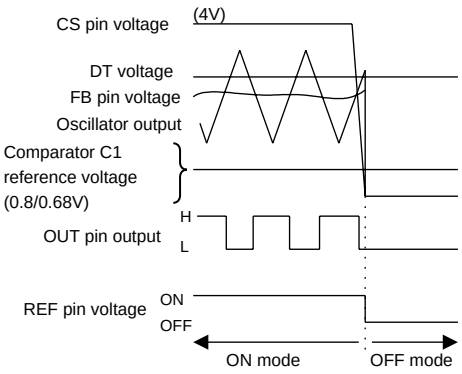


Fig. 12 Output ON/OFF control circuit timing chart

4. Overcurrent limiting circuit

The overcurrent limiting circuit detects the peak value of every drain current pulse (pulse by pulse method) of the main switching MOSFET to limit the overcurrent. The detection threshold voltage is +0.24V for FA5510/11 or –0.17V for FA5514/15 with respect to the ground as shown in Figure 13 and Figure 14. The drain current of the MOSFET is converted to voltage by resistor Rs and fed to the IS pin of the IC. If the voltage exceeds the reference voltage +0.24V (FA5510/11) or –0.17V (FA5514/15) of comparator C4, comparator C4 works to set flip-flop output Q to high. The output is immediately turned off to shut off the current. Flip-flop output Q is reset on the next cycle to turn on the output again. This operation is repeated to limit the overcurrent.

If the overcurrent limiting circuit malfunctions due to noise, place an RC filter between the IS pin and MOSFET as shown in Figure 13 and Figure 14. (See item 12 in “Design advice.”) Figure 15 is a timing chart that illustrates overcurrent-limiting operations.

5. Vcc overvoltage protection circuit

The IC contains a Vcc overvoltage protection circuit to protect the IC from damage by overvoltage. Figure 16 shows the overvoltage protection circuit. Figure 17 is a timing chart that illustrates overvoltage protection operations. Overvoltage is detected if the supply voltage Vcc rises to 31.8V (Icc=14mA) or more and current flows in the built-in zener diode. The output of comparator C5 then goes high and the constant current source (0.95mA) raises the CS pin voltage. When the CS pin voltage exceeds 8.5V, the output of comparator C2 goes high to turn off the 5V REF circuit. The IC then enters the latched mode and the IC output is put in the off (low voltage) state. When latched mode, the IC current consumption is 45µA (typ) (Vcc=10V). This current must be supplied through the startup resistor.

The overvoltage shutdown operation can be reset by lowering the supply voltage to below 9.0V or forcing the CS pin voltage below 7.9V. (When you want to enable Vcc overvoltage shutdown at a desired voltage, see item 6 in “Design advice.”)

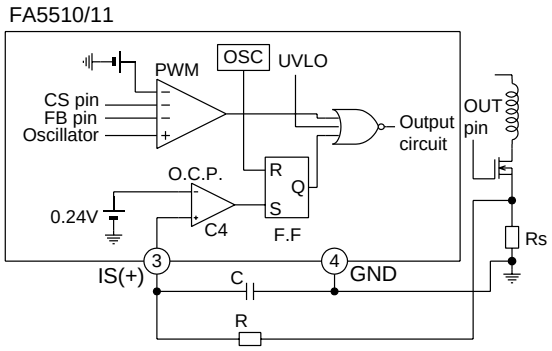


Fig. 13 Overcurrent limiting circuit (FA5510/11)

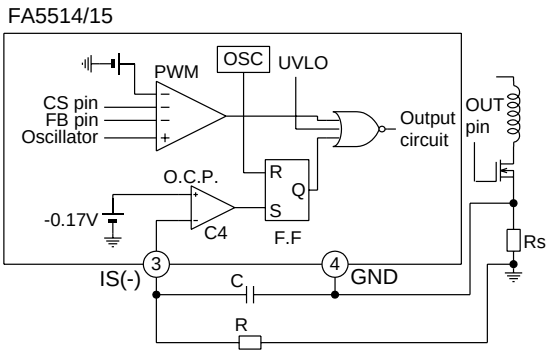


Fig. 14 Overcurrent limiting circuit (FA5514/15)

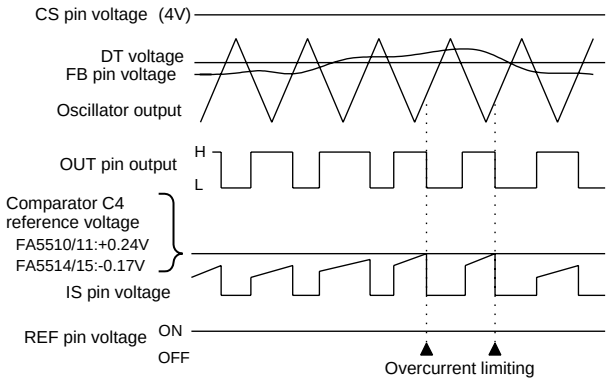


Fig. 15 Overcurrent timing chart

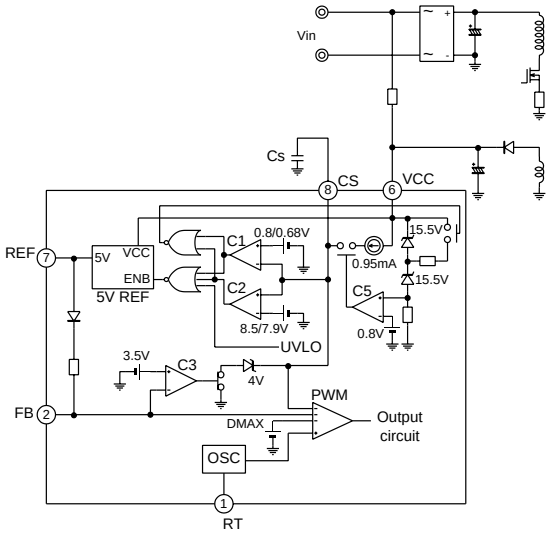


Fig. 16 Overvoltage shutdown circuit

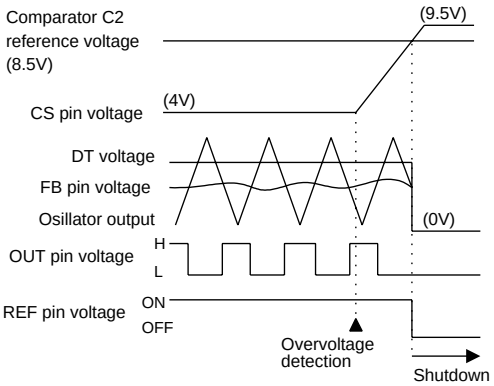


Fig. 17 Overvoltage shutdown timing chart

6. Undervoltage lockout circuit (U.V.L.O.)

The IC incorporates a circuit that prevents the IC from malfunctioning when the supply voltage drops. When the supply voltage is raised from 0V, the IC starts operation with Vcc=16.5V (typ). If the supply voltage drops, the output is shut down when Vcc=9.0V (typ). When the undervoltage lockout circuit operates, the outputs of the OUT and CS pins go low to reset the IC.

7. Output circuit

The IC contains a push-pull output stage and can directly drive the MOSFET. The absolute maximum rating of OUT pin peak current is ±1.5A. But when using in actual circuit, the output peak current depends on the characteristics of the MOSFET, resistance between the OUT pin and the MOSFET, supply voltage, temperature and so. When supply voltage is relatively low or temperature is relatively high, the output peak current may not reach the maximum ratings.

Note that the output current causes loss of the output stage. The total loss caused by the operating current and the output current should be within the ratings in actual circuit.

■ Design advice

1. Deciding the startup circuit

These ICs, which use CMOS process, consume less current, and therefore can use larger startup resistance than the conventional bipolar type of IC. To decide the startup resistance, the following conditions must be satisfied:

(a) The IC is started when the power is turned on.
(b) The IC consumption current is supplied during latch mode operation to maintain the latch state.
(c) The IC consumption current is supplied during the off state under the on/off function to maintain the off state.

However, these are the minimum conditions for using the IC. The startup time required for the power supply must also be decided on.

1.1 Connecting the startup resistor before rectification (AC line)

When the startup resistor is connected before rectification (AC line) as shown in Figure 18, the voltage applied to the startup resistor forms a half-wave rectified waveform of the AC input voltage. Startup resistor R1 must satisfy the three equations shown below. Select a smaller-side value for R1 in consideration of the temperature characteristics.

(a) To supply startup current 30µA at ON threshold voltage 17.5V (max.) of UVLO:

$$R1 < \frac{\frac{\sqrt{2}}{\pi} \times Vac - 17.5}{0.03} \quad \cdots\cdots (5)$$

(b) To supply IC consumption current 80µA (max.) (Vcc=10V) in latch mode:

$$R1 < \frac{\frac{\sqrt{2}}{\pi} \times Vac - 10}{0.08} \quad \cdots\cdots (6)$$

(c) To supply IC consumption current 200µA (max.) (Vcc=17V) in the off state under the on/off function:

$$R1 < \frac{\frac{\sqrt{2}}{\pi} \times Vac - 17}{0.2} \quad \cdots\cdots (7)$$

R1: Startup resistance [kΩ]
Vac: Effective value of AC input voltage [V]

If neither the latch mode operation nor the on/off functions are used, only the expression in (5) needs to be satisfied. In this method, the supply current to the IC via the start-up resistor is stopped when AC input is shut down. Therefore, after latch mode operation, shutting the AC input down resets the latch mode in a very short period of time.

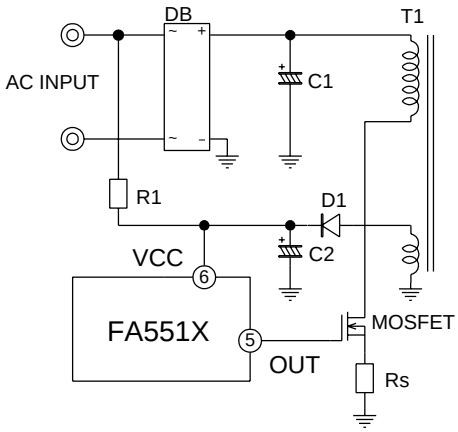


Fig. 18 Startup circuit (1)

1.2 Connecting the startup resistor after rectification (DC line)

When the startup resistor is connected after rectification (DC line) as shown in Figure 19, the voltage applied to the startup resistor becomes the peak value of the AC input voltage. Startup resistor R1 must satisfy the three equations shown below. Select a smaller-side value for R1 in consideration of temperature characteristics.

(a) To supply startup current 30µA at ON threshold voltage 17.5V (max.) of UVLO:

$$R1 < \frac{\sqrt{2} \times Vac - 17.5}{0.03} \quad \text{..... (8)}$$

(b) To supply IC consumption current 80µA (max.) (Vcc =10V) in latch mode:

$$R1 < \frac{\sqrt{2} \times Vac - 10}{0.08} \quad \text{..... (9)}$$

(c) To supply IC consumption current 200µA (max.) (Vcc = 17V) in the off state under the on/off function:

$$R1 < \frac{\sqrt{2} \times Vac - 17}{0.2} \quad \text{..... (10)}$$

R1: Startup resistance [kΩ]
Vac: Effective value of AC input voltage [V]

If neither the latch nor the on/off functions are used, only the expression in (8) needs to be satisfied. In this method, after latch mode operation, smoothing capacitor C1 in the main circuit supplies current to the IC via the startup resistor even if the AC input is shut down. Therefore, some time must elapse before the latch mode is reset.

2. Determining the Vcc capacitor value

To properly start the power supply, a certain value is required for the capacitor connected to the VCC pin. Figure 20 shows the Vcc voltage at start-up when a proper value is given to the capacitor. When the input power is turned on, the capacitor connected to the VCC pin is charged via the startup resistor and the voltage increases. The IC is then in standby state and almost no current is consumed. (Icc<2µA) Thereafter, Vcc reaches the ON threshold voltage of UVLO and the IC begins operation. When the IC begins operation to make output, the IC operates based on the voltage from the auxiliary winding. When the IC is just starting up, however, it takes time for the voltage from the auxiliary winding to rise enough, and Vcc drops during this period.
Determine the Vcc capacitor value so that Vcc will not drop down to the OFF threshold voltage of UVLO during this period.

If the Vcc capacitor value is too small, Vcc will drop to the OFF threshold voltage of UVLO before the auxiliary winding voltage rises enough. If so, Vcc repeatedly goes up and down between the UVLO threshold voltages, and the power supply cannot start up. (Figure 21)

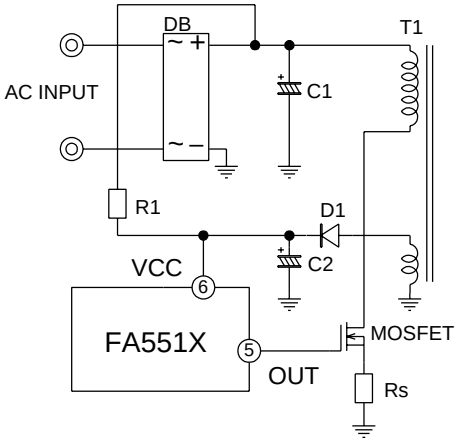


Fig. 19 Startup circuit (2)

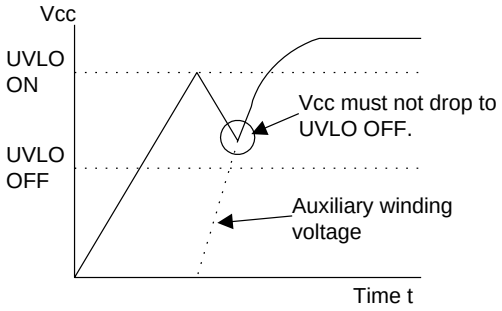


Fig. 20 Vcc voltage at startup with a adequate capacitor

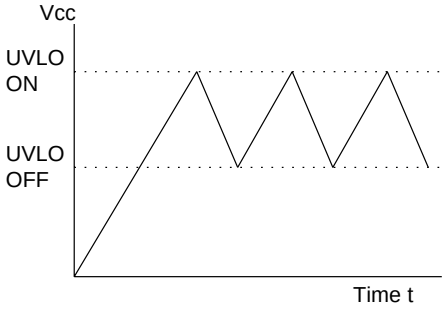


Fig. 21 Vcc voltage at startup with a inadequate capacitor

3. The startup period

The start up period from the time the power is on to the time the IC is turn to on is approximately given by:

$$t_{start\text{-}up} = -C2 \times R1 \times \ln\left(1 - \frac{16.5}{V1}\right) \quad \cdots\cdots (11)$$

Where:
R1: Startup resistor [Ω]
C2: Capacitor between VCC and GND pin [F]
Vac: Effective value of AC input voltage [V]

$$V1 = \begin{cases} \dfrac{\sqrt{2} \times Vac}{\pi} & \text{.....(Connecting a startup resistor before rectification)} \\ \sqrt{2} \times Vac & \text{..... (Connecting a startup resistor after rectification)} \end{cases}$$

To shorten the start-up period, the capacitor C2 or resistor R1 should be decreased. But in some case, such as when the load current of the power supply is changed rapidly, you may want to prolong the hold time of the Vcc voltage over the off threshold. In this case the capacitor C2 cannot be decreased and the resistor R1 should be decreased. But loss of the resistor R1 increases.
In such case, the circuit shown in Fig. 23 is effective to shorten start-up period without increasing the loss of the resistor R1. The capacitor C2 is decreased to shorten the start-up period and, after the IC starts up, Vcc voltage supplied from C3 to prolong the hold time of the Vcc voltage.
The start-up period of this circuit also is approximately given by the expression in (11)

4. Setting soft start period and OFF latch delay independently

Figure 24 shows a circuit for setting the soft start period and OFF latch delay independently. In this circuit, capacitance C_S determines the soft start period, and capacitance C_L determines the OFF latch delay. If the overload shutdown or overvoltage shutdown functions raise the CS pin voltage to around 5V, zener diode Zn becomes conductive to charge capacitor C_L. The OFF latch delay can be thus prolonged by capacitance C_L.

5. Overvoltage protection using the VCC pin

These ICs contain an overvoltage protection function detecting the Vcc voltage using internal ZD (See item 5 in “Description of each circuit”). If Vcc voltage exceed 31.8V, the current of 14mA flows through the internal ZD and the overvoltage protection function operates.
After this protection function operates, the IC continues to consume the large current if high voltage continues to be applied to the Vcc pin. Mind that total IC loss does not exceed the rating. If the voltage source applied to Vcc pin has relatively high impedance and cannot supply the current of 14mA, overvoltage protection function does not operate. But the internal ZD maintains the Vcc voltage 32V or less and protects the IC.

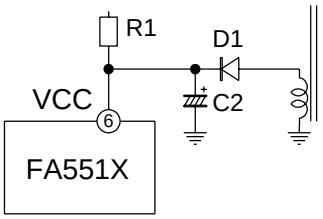


Fig. 22 Startup circuit (3)

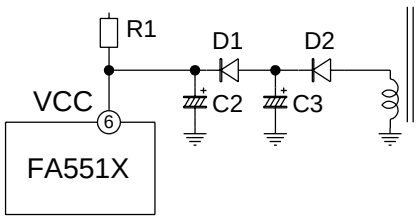


Fig. 23 Startup circuit (4)

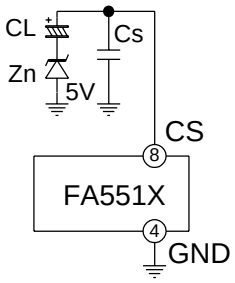


Fig. 24 Independent setting of soft start period and OFF latch deley

6. Overvoltage protection using CS pin

These ICs contain the overvoltage protection function detecting Vcc voltage. However, the threshold voltage is fixed. Adding a circuit to CS pin enables the overvoltage protection detecting desired voltage.

6.1 Detecting on secondary side

Figure 25 shows the overvoltage shutdown circuit based on the signal from the secondary side. The optocoupler output transistor is connected between the CS and VCC pins. When the output voltage is put in the overvoltage state, the optocoupler output transistor goes on to raise the CS pin voltage via resistor R2. When the CS pin voltage exceeds the reference voltage (8.5V) of internal comparator, the IC enters the OFF latch mode and shuts the output down. The IC consumes current 45µA (typ) (Vcc=10V) in latch mode. This current must be supplied via startup resistor R1. The overvoltage protection circuit can be reset by lowering the supply voltage Vcc to below 9.0V or forcing the CS pin voltage below 7.9V. In normal operation, the CS pin voltage is clamped by the 4V zener diode with maximum sink current 45µA . Therefore, to raise the CS pin voltage to 8.5V or more, 45µA or a higher current needs to be supplied from the optocoupler. Set the current input to the CS pin to 1mA or less.

6.2 Detecting on primary side (detecting Vcc voltage)

To attain overvoltage protection, the CS pin voltage is forcibly raised from outside the IC until it exceeds the reference voltage (8.5V) of the internal comparator C2. When the reference voltage is exceeded, the IC enters latch mode and shuts the output down. Connect a zener diode (ZD) and resistor between the VCC and CS pins as shown in Figure 26. When the Vcc voltage exceeds about ZD voltage +8.5V, the IC enters the OFF latch mode and shuts the output down. If Vcc remains high even after shutdown and current is input to the CS pin, set the current to 1mA or lower. Set the zener voltage of the ZD connected to the CS pin higher than the UVLO ON threshold voltage. Startup is disabled below this voltage.

Figure 27 shows another circuit for enabling latch mode shutdown by detecting a desired Vcc voltage using the CS pin. In this circuit, overvoltage shutdown works when the Vcc voltage is about the same as the ZD voltage. For this circuit also, use a ZD voltage higher than the UVLO ON threshold voltage. Set the current flowing into the CS pin to 1mA or lower.

7. Feedback pin circuit

Figure 28 gives an example of connection in which a feedback signal is input to the FB pin. If this circuit causes power supply instability, connect R3 and C4 as shown in Figure 28 to decrease the frequency gain. Set R3 between several tens of ohms to several kilohms and C4 between several thousand picofarads to one microfarad.

If noise is applied to the FB pin, the output pulses may be lacked or disturbed.
In this case, connect a capacitor C5 as shown in Fig. 29 to suppress the noise applied to the FB pin. Set the capacitance of C5 less than 10% of capacitance of C4 and connect C5 as near the IC as possible.

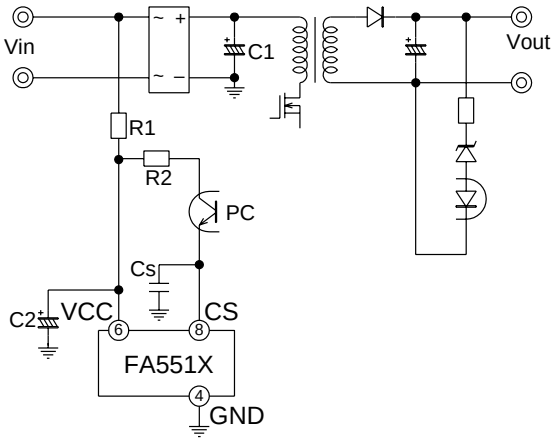


Fig. 25 Overvoltage shutdown circuit (1)

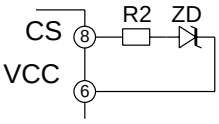


Fig. 26 Overvoltage shutdown circuit (2)

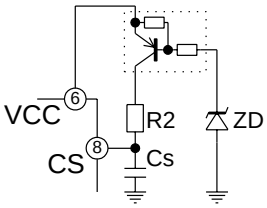


Fig. 27 Overvoltage shutdown circuit (3)

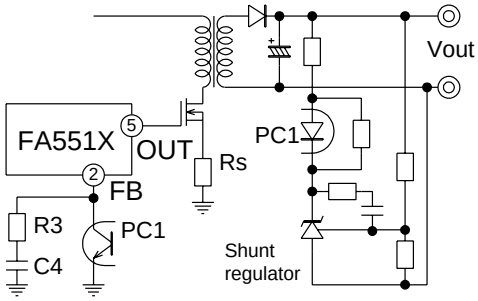


Fig. 28 FB pin circuit (1)

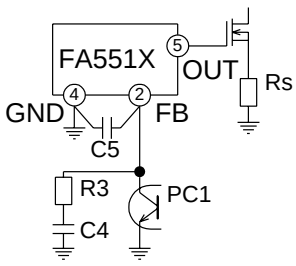


Fig. 29 FB pin circuit (2)

8. Simple voltage control on the primary side

In a flyback type power supply, the output voltages of the power supply and auxiliary winding voltage are almost proportional to the number of winding turns of the transformer. This characteristic can be used in the circuit shown in Figure 30, where the output voltage can easily be made constant by detecting the auxiliary winding voltage.

However, this is an easy output voltage control method, and the output voltage precision and regulation are therefore not as good.

To reduce output pulse width completely to 0%, the FB pin voltage must fall below 0.9V and R5 must be set below about 1kΩ from the characteristics of the FB pin voltage and source current.

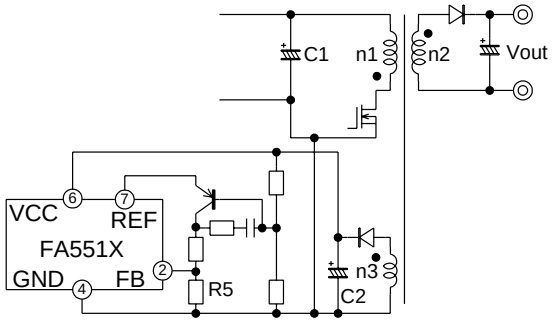


Fig. 30 Simple voltage control circuit

9. Disabling the overload shutdown function

As shown in Figure 31, connect a 10kΩ resistor R6 between the FB pin and the ground. The FB pin voltage then does not rise sufficiently high to reach the shutdown threshold voltage when an overload occurs so that IC does not enter OFF latch mode. Use a 5% or better-precision resistor for R6.

Even with this connection, the overvoltage shutdown function is available.

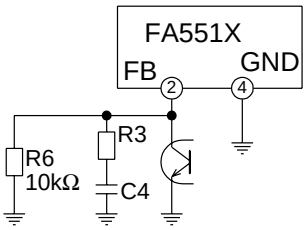


Fig. 31 Disabling overload shutdown function

10. Polarities for overcurrent detecting and their characteristics

The FA5510/11 uses positive polarity detection for overcurrent limiting (number 3 pin of IS pin) and the FA5514/15 uses negative polarity detection. The characteristics of positive and negative polarity detection are summarized below. Select one in accordance with the circuit used. (See item 4 in "Description of each circuit.")

Positive detection (FA5510/11)

- Wiring is easy because the ground can be shared by the main circuit and IC peripherals.
- It is easy to correct the current detected as overload against the input voltage.

Negative detection (FA5514/15)

- The MOSFET drive current does not flow to the current detection resistor and therefore it hardly affects overcurrent detection.

11. Correcting overload detection current (FA5510/11 only)

If the power supply output is overloaded, the overcurrent limiting function restricts the output power and the overload shutdown function stops the IC. The output current when an overload occurs varies depending on the input voltage; the higher the input voltage, the more the overload detection current may increase. If any problems occur as a result of the appearance of this symptom, connect resistor R8 between current detection resistor Rs and the IS (+) pin and add resistor R7 for correction as shown in Figure 32. The standard resistance of R8 is several hundred ohms, and that of R7 is from several hundred kilohms to several megohms.

Note that the above correction slightly lowers the output current when overload even where the input voltage is low. This correction is available only for the FA5510/11 that uses positive polarity for overcurrent detection.

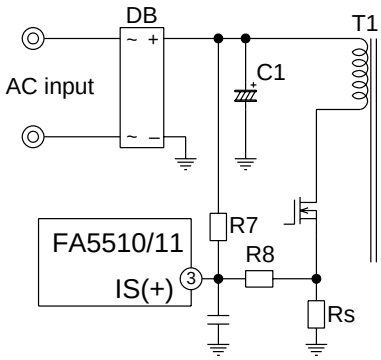


Fig. 32 Correction of overload detection current

12. Preventing malfunction caused by noise

Noise applied to each pin may cause malfunction of the IC. If noise causes malfunction, see the notes summarized below and confirm in actual circuit to prevent malfunction.

- The IS pin for overcurrent limiting function detects the MOSFET current converted to the voltage. The parasitic capacitor and inductor of the MOSFET, transformer, wiring, etc. cause a noise in switching operation. If this switching noise causes a malfunction of overcurrent limitimg function, insert the RC filter into IS pin as shown in Figure 13 and 14. Connect this capacitor as near the IC as possible to suppress noise effectively.

- Connect a noise prevention capacitor (0.1µF or more) to the REF pin that outputs the reference voltage for each component.

- If noise is applied to the FB pin, the output pulses may be disturbed. In this case, see item 7 in “Design advice.”

- Relatively large noise may occur at the VCC pin because large current flows from VCC pin to drive the MOSFET. Then this noise may cause malfunction of the IC. In addition, the IC may stop operation when Vcc voltage drops below the off threshold voltage by noise. Mind that capacitance and characteristics of the capacitor connected between VCC and GND pin not to allow the large noise at the VCC pin. To prevent malfunction, suppress the noise width below about 0.5µs or less and noise voltage below about ±0.6V or less.

13. Preventing malfunction caused by negative voltage applied to a pin

When large negative voltage is applied to each IC pin, a parasitic element in the IC may operate and cause malfunction. Be careful not to allow the voltage applied to each pin to drop below –0.3V. Especially for the OUT pin, voltage oscillation caused after the MOSFET turns off may be applied to the OUT pin via the parasitic capacitance of the MOSFET, causing the negative voltage to be applied to the OUT pin. If the voltage falls below –0.3V, add a Schottky diode between the OUT pin and the ground. The forward voltage of the Schottky diode can suppress the voltage applied to the OUT pin. Use the low forward voltage of the Schottky diode.

Similarly, be careful not to cause the voltages at other pins to fall below –0.3V.

14. Gate circuit configuration

To adjust switching speeds or prevent oscillation at gate terminals, resistors are normally inserted between the power MOSFET gate terminal to be driven and the OUT pin of the IC. You may prefer to decide on the drive current independently, to turn the MOSFET on and off. If so, connect the MOSFET gate terminal to the OUT pin of the IC as shown in Figure 34. In this circuit, Rg1 and Rg2 restrict the current when the MOSFET is turned on, and only Rg1 restricts the current when it is turned off.

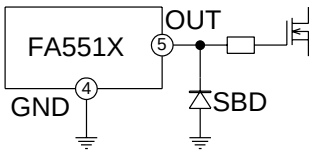


Fig. 33 Protection of OUT pin against the negative voltage

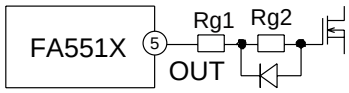


Fig. 34 Gate circuit

15. Loss calculation

IC loss must be confirmed to use the IC within the ratings. Since it is hard to directly measure IC loss, some examples of calculating approximate IC loss are given below.

15.1 Calculation example 1

Suppose the supply voltage is Vcc, IC current consumption is Iccop, the total gate charge of the power MOSFET is Qg, and the switching frequency is fsw. Total IC loss Pd can be calculated by:

$$Pd \fallingdotseq Vcc \times (Iccop + Qg \times fsw) \quad \cdots\cdots (12)$$

This expression calculates an approximate value of Pd, which is normally a little larger than the actual loss. Since various conditions such as temperature characteristics apply, thoroughly verify the appropriateness of the calculation under all applicable conditions.

Example:
When Vcc=18V, Iccop=2.5mA (max.) is obtained from the specifications. Suppose Qg=80nC and fsw=100kHz.

$$Pd \fallingdotseq 18V \times (2.5mA + 80nC \times 100kHz)$$
$$\fallingdotseq 189mW$$

15.2 Calculation example 2

The IC loss consists of the loss caused by operation of the control circuit and the loss caused at the output circuit to drive the power MOSFET.

15.2.1 Loss at the control circuit

The loss caused by operation of the IC control circuit is calculated by the supply voltage and IC current consumption. When the supply voltage is Vcc and IC current consumption is Iccop, loss Pop at the control circuit is:

$$Pop = Vcc \times Iccop \quad \cdots\cdots (13)$$

Example:
When Vcc=18, Iccop=1.9mA (typ) is obtained from the specifications. The typical IC loss is given by:

$$Pop = 18V \times 1.5mA = 27mW$$

15.2.2 Loss at the output circuit

The output circuit of the IC is a MOSFET push-pull circuit. When the ON resistances of MOSFETs making up the output circuit are Ron and Roff, the resistances can be determined as shown below based on Vcc=18V and Tj = 25°C obtained from the output characteristics shown in the specifications:

Ron = 15Ω (typ), Roff=7Ω (typ)

When the total gate charge of the power MOSFET is Qg, the switching frequency is fsw, the supply voltage is Vcc, and gate resistance is Rg, the loss caused at the IC output circuit is given by:

$$Pdr = \frac{1}{2} \times Vcc \times Qg \times fsw \times \left(\frac{Ron}{Rg + Ron} + \frac{Roff}{Rg + Roff} \right) \quad \cdots\cdots (14)$$

When gate resistance differs between ON and OFF as shown in Figure 36, the loss is given by:

$$Pdr = \frac{1}{2} \times Vcc \times Qg \times fsw \times \left(\frac{Ron}{Rg1+Rg2+Ron} + \frac{Roff}{Rg1+Roff} \right) \quad \cdots\cdots (15)$$

Example:
When Vcc=18V, Qg=80nC, fsw=100kHz, and Rg=10Ω, the typical IC loss is given by:

$$Pdr = \frac{1}{2} \times 18V \times 80nC \times 100kHz \times \left(\frac{15\Omega}{10\Omega+15\Omega} + \frac{7\Omega}{10\Omega+7\Omega} \right)$$

$$= 72.8mW$$

15.2.3 Total loss

The total loss (Pd) of the IC is the sum of the control circuit loss (Pop) and the output circuit loss (Pdr) calculated previously:

$$Pd = Pop + Pdr \quad \cdots\cdots (16)$$

Example:
The standard IC loss under the conditions used in (1) and (2) above are:

Pd = Pop + Pdr = 27mW + 72.8mW = 99.8mW

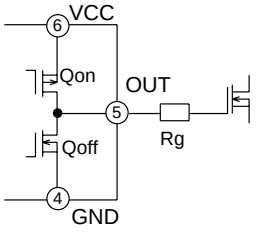


Fig. 35 Output Circuit (1)

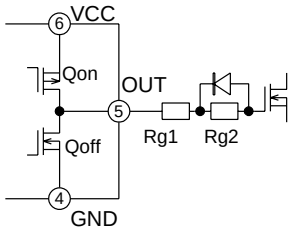
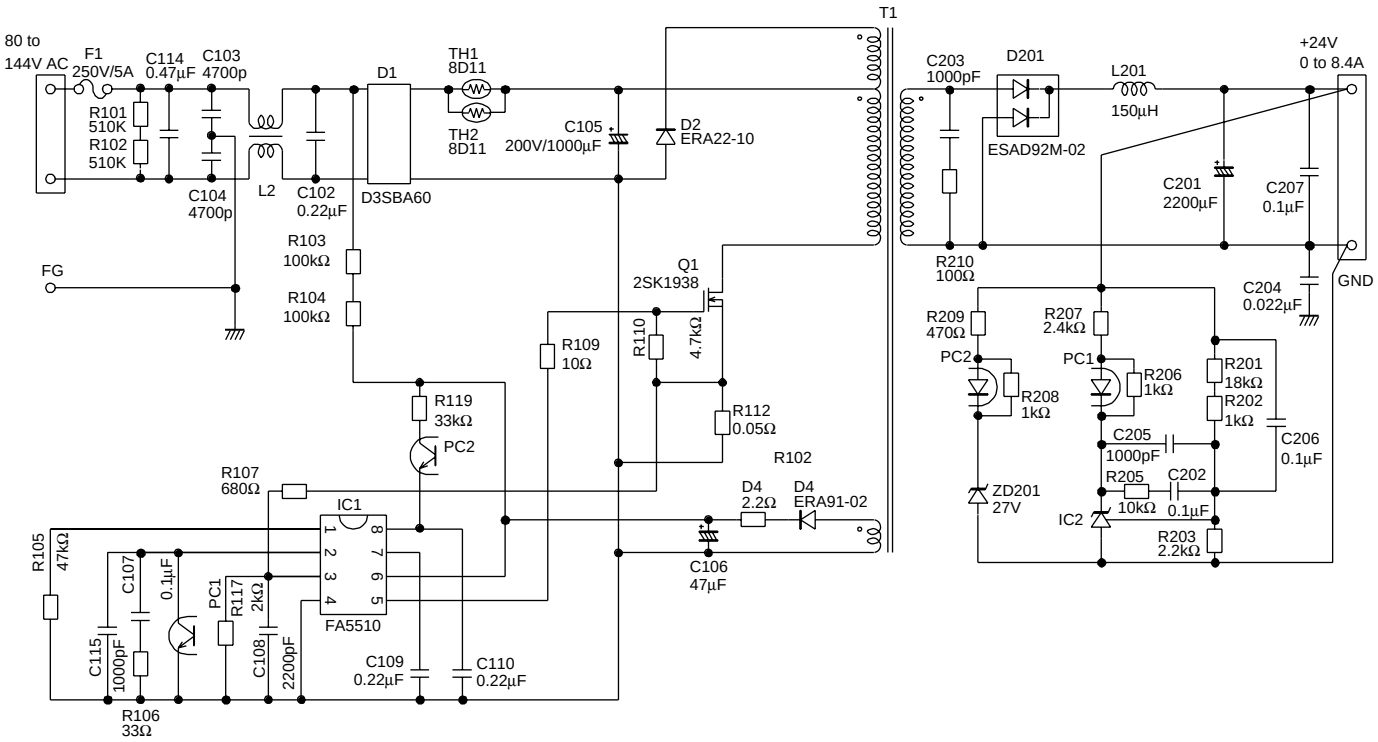


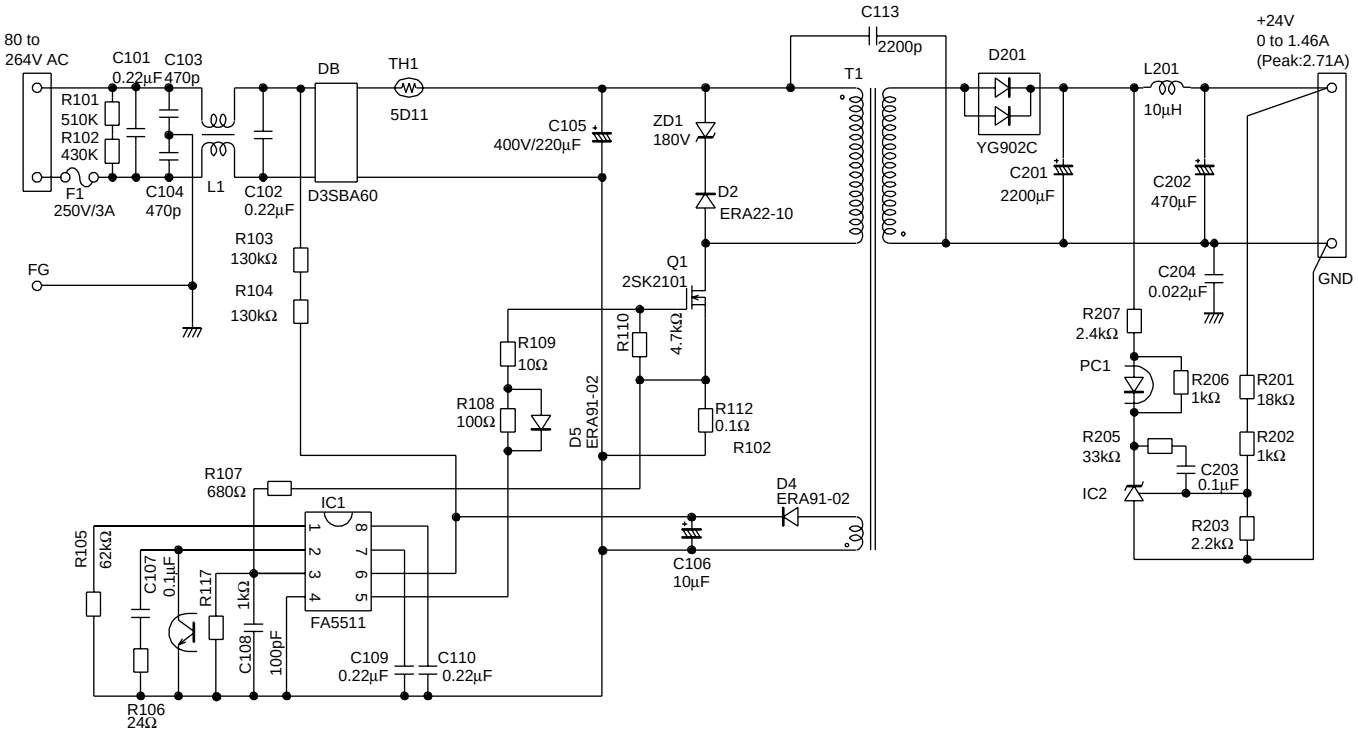
Fig. 36 Output Circuit (2)

■ Application circuit

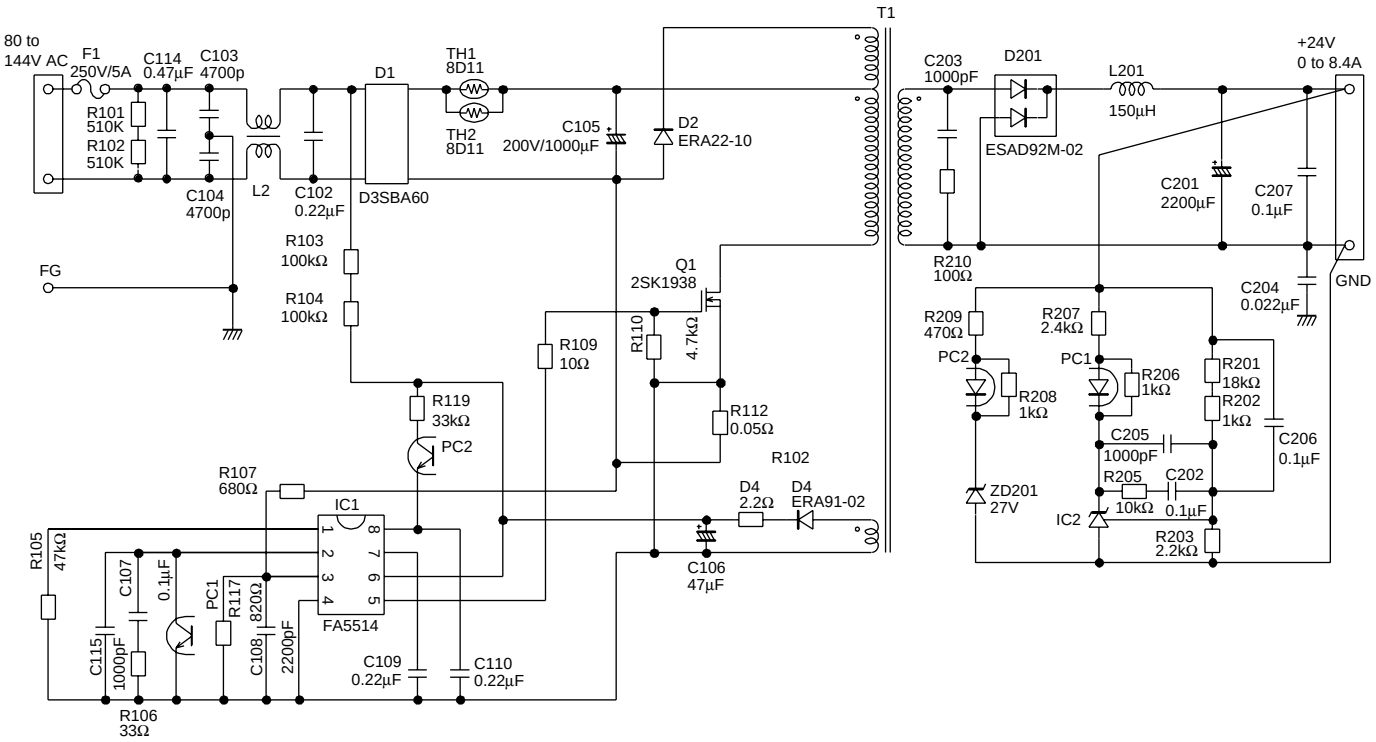
● FA5510



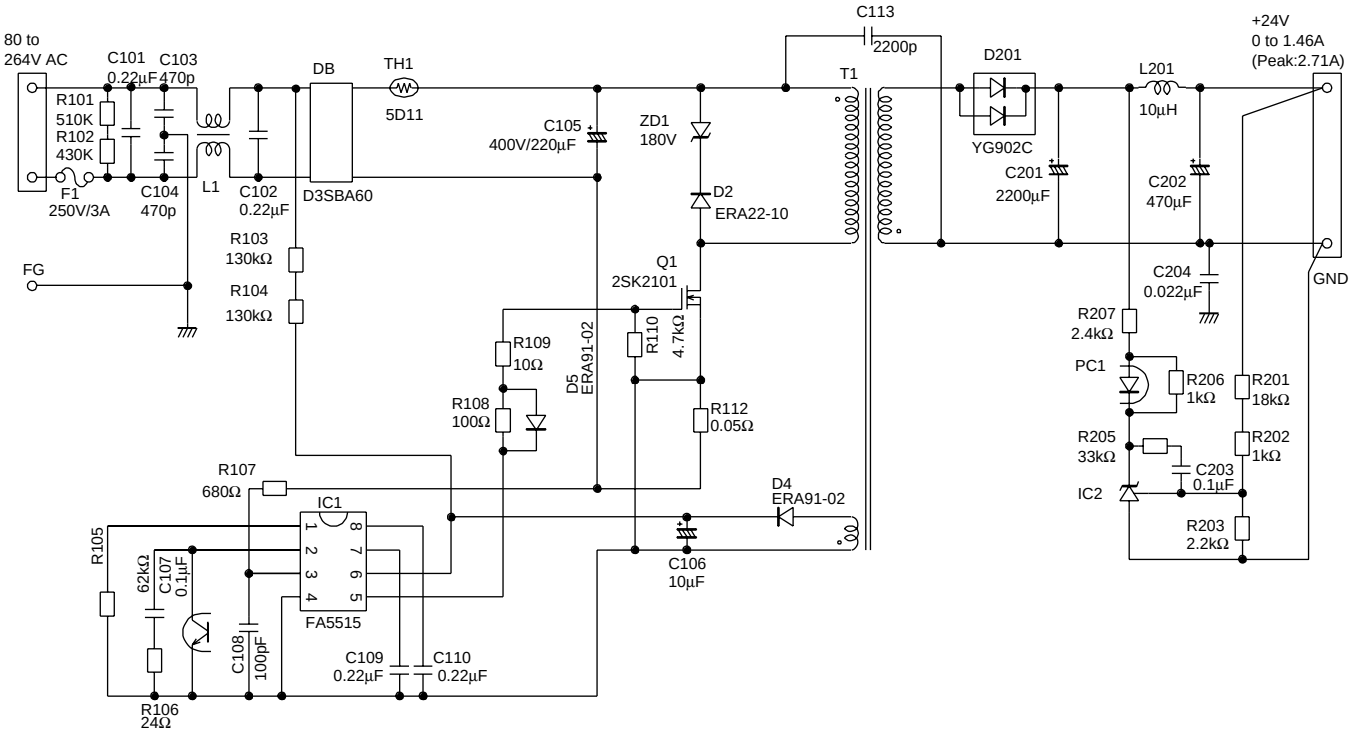
● FA5511



● FA5514



● FA5515



Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.