FT5x16

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT5x16 Series ICs are single-chip capacitive touch panel controller ICs with a built-in Micro-controller unit (MCU).They adopt the mutual capacitance approach, which supports true multi-touch capability. In conjunction with a mutual capacitive touch panel, the FT5x16 have user-friendly input functions, which can be applied on many portable devices, such as cellular phones, MIDs and GPS.

The FT5x16 series ICs include FT5216/FT5316, the difference of their specifications will be listed individually in this datasheet.

FEATURES

- Mutual Capacitive Sensing Techniques
- True Multi-touch with up to 5 Points of Absolution X and Y Coordinates
- Immune to RF Interferences
- Auto-calibration: Insensitive to Capacitance and Environmental Variations
- FT5216 supports up to 16 TX lines + 10 RX lines
- FT5316 supports up to 21 TX lines + 12 RX lines
- Full Programmable Scan Sequences to Support Various TX/RX Configurations
- High Report Rate: More than 100Hz
- Touch Resolution of 100 Dots per Inch (dpi) or above -- depending on the Panel Size
- Optional Interfaces :I2C/SPI
- 2.8V to 3.6V Operating Voltage
- IOVCC Connected to External or Internal 1.8V to 3.6V Voltage Supply for Digital IO Circuits
- Capable of Driving Single Channel (transmit/receive) Resistance: Up to10K Ω
- Capable of Supporting Single Channel (transmit/receive) Capacitance: 60 pF
- Optimal Sensing Mutual Capacitor: 1pF~4pF
- 12-Bit ADC Accuracy
- Built-in Enhanced MCU
- 3 Operating Modes
  - Active
  - Monitor
  - Hibernate
- Operating Temperature Range: -20°C to +85°C

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT5x16 accommodate a wide range of applications with a set of buttons up to a 2D touch sensing device, their typical applications are listed below.

- Mobile phones, smart phones
- MIDs
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT5x16 Series ICs support < 5.0" Touch Panel, users may find out their target IC from the specs. listed in the following table,

Model Name	Panel		Package			Touch Panel Size	Recommended Pitch
	TX	RX	Type	Pin	Size		
FT5216GM7	16	10	QFN5*5	40	0.75-P0.4	<3.6"	~5mm
FT5316DME	21	12	QFN6*6	48	0.75-P0.4	3.7"～5.0"	~5mm

Remarks: FocalTech suggests to use pitch between 4.0mm to 6.0mm; The customer can decide the pitch based on applications.

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT5x16.

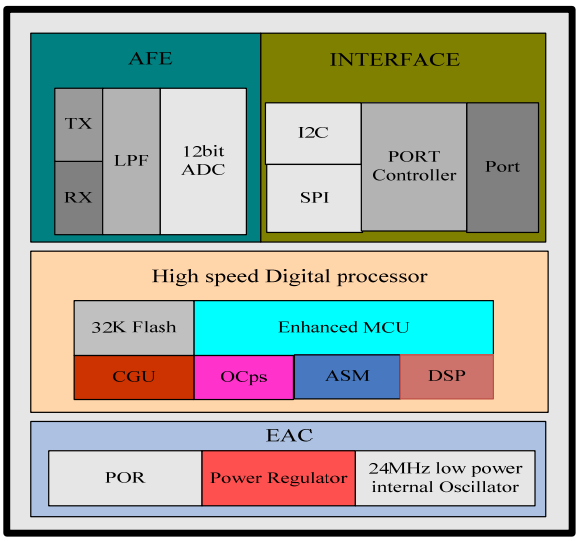


Figure 2-1 FT5x16 System Architecture Diagram

The FT5x16 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So, it supports both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces, which will be explained in detail in a later section.

- Enhanced MCU with DSP accelerator

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash ROM is implemented to store programs and some key parameters.
Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably. Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C/SPI: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RESETN: an external low signal reset the chip. the port is also use to wakeup the FT5x16 from the Hibernate mode.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.

2.2 MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- Program Memory: 32KB Flash
- Data Memory: 4KB SRAM
- A DSP accelerator is cooperate with MCU to process the Complex algorithms
- Timer: A number of timers are available to generate different clocks
- Master Clock: 24MHz
- Clock Manager: To control various clocks under different operation conditions of the system

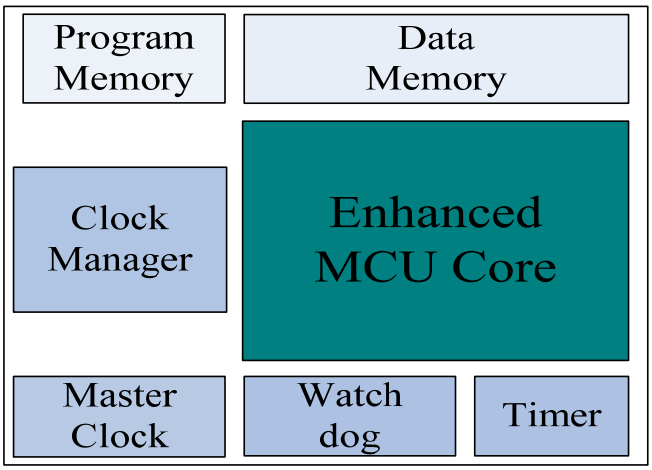


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT5x16 operates in the following three modes:

- Active Mode

When in this mode, FT5x16 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT5x16 to speed up or to slow down.

- Monitor Mode

When in this mode, FT5x16 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine

if there is a touch or not. When a touch is detected, FT5x16 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- Hibernate Mode

In this mode, the chip is set in a power down mode. It shall only respond to the "WAKE" or "RESET" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4 Host Interface

Figure 2-3 shows the interface between a host processor and FT5x16. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5x16 to the Host
- Reset Signal from the Host to FT5x16

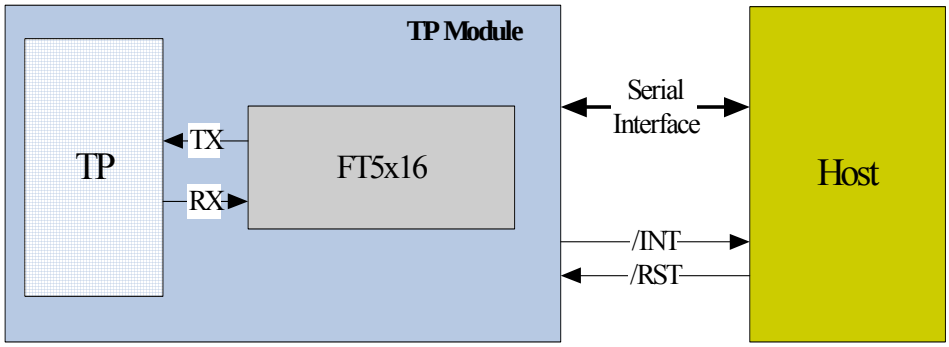


Figure 2-3 Host Interface Diagram

The serial interfaces of FT5x16 is I2C or SPI. The details of this interface are described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5x16 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to reset FT5x16 from the Hibernate mode. After resetting, FT5x16 shall enter the Active mode.

2.5 Serial Interface

FT5x16 supports the I2C or SPI interfaces, which can be used by a host processor or other devices.

2.5.1 I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

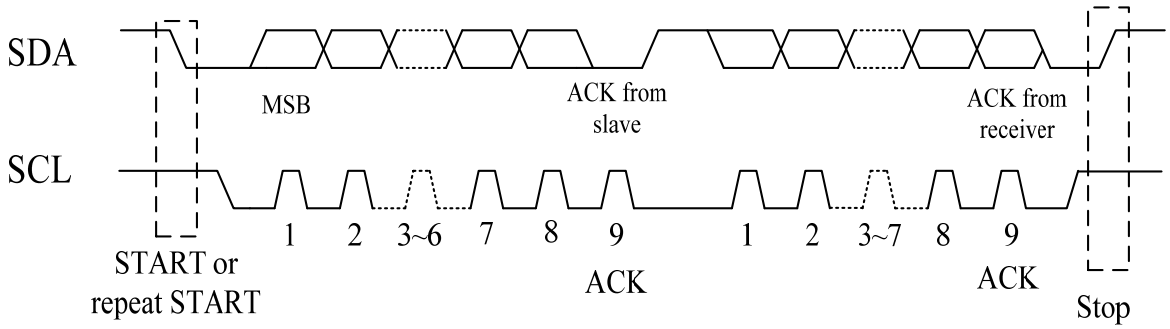


Figure 2-4 I2C Serial Data Transfer Format

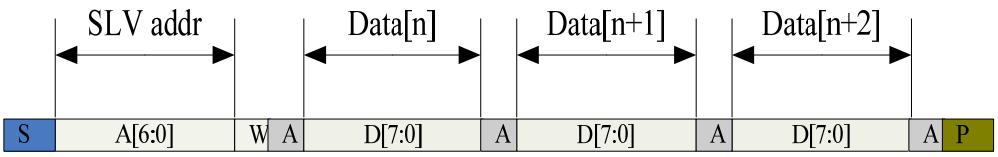


Figure 2-5 I2C master write, slave read

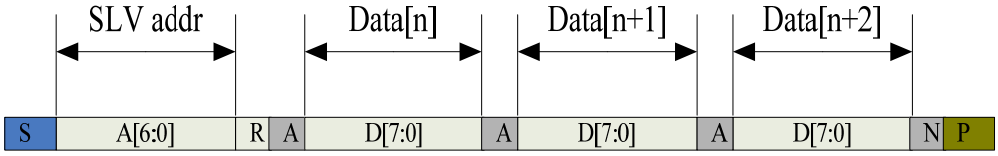


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:0]: address bits are identical to those of I2CADDR [7:1] register.
R/ W	'1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

2.5.2 SPI

SPI is a 4 wire serial interface. The following is a list of the 4 wires:

- SCK: serial data clock
- MOSI: data line from master to slave
- MISO: data line from slave to master
- SLVESEL: active low select signal

SPI transfers data at 8bit packets. The phase relationship between the data and the clock can be defined by the two registers: phase and polck. Some data transfer examples can be found in Figure 2-7 to Figure 2-10.

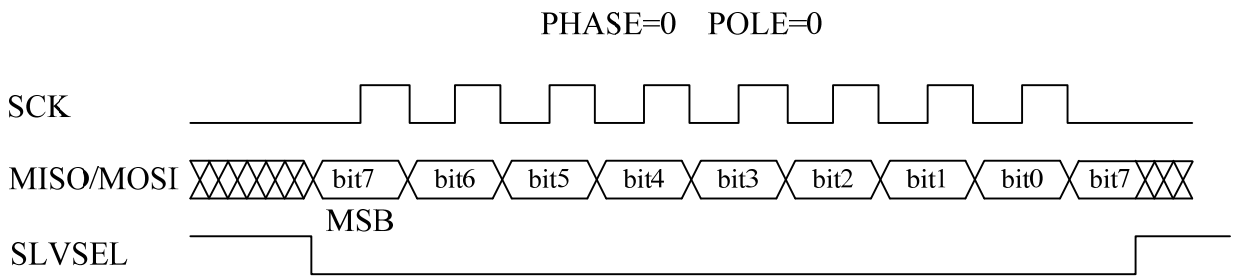


Figure 2-7 SPI Data Transfer Format (Phase=0, POLCK=0)

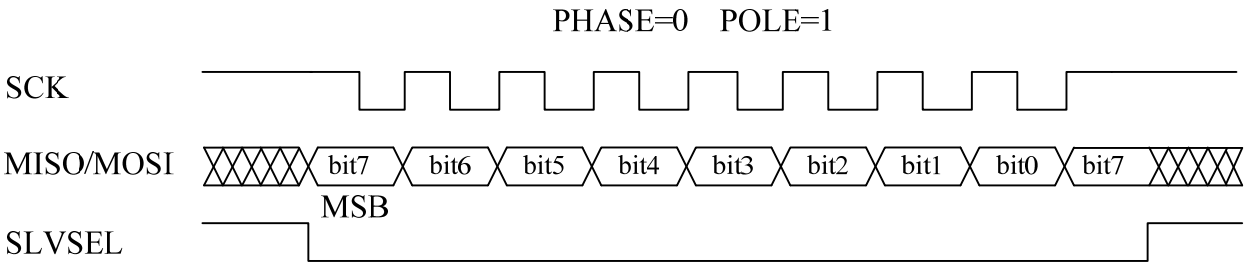


Figure 2-8 SPI Data Transfer Format (PHASE=0, POLCK=1)

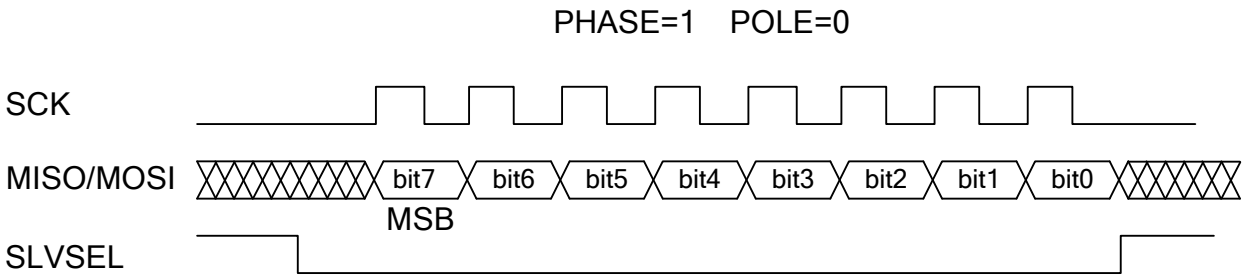


Figure 2-9 SPI Data Transfer Format (Phase=1, POLCK=0)

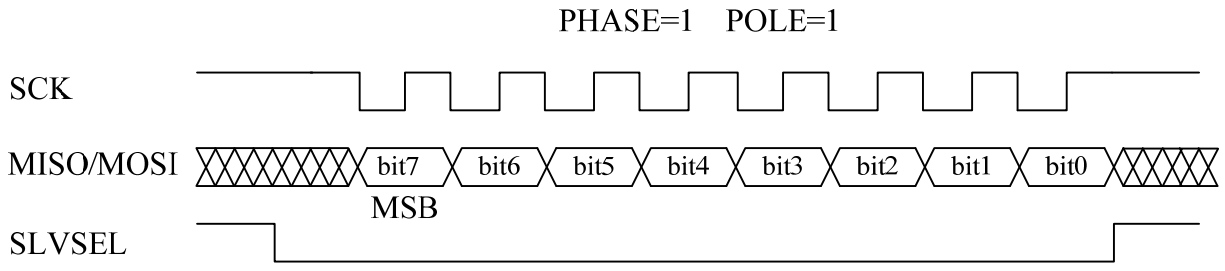


Figure 2-10 SPI Data Transfer Format (Phase=1, POLCK=1)

SPI can be configured into either Master or Slave mode via the MAS bit of the SPI0CON register. When in the Master mode, the SPI needs to supply the data clock, whose frequency relationship with the Master clock can be set by CLKDVD bits of the SPI0CON register. When it is configured in the Slave mode, the clock, SCK, is supplied by the external Master. The maximum data clock frequency must not be higher than $\frac{F_{mclk}}{8}$.

SPI Interface Timing Characteristics is shown in the following Figure2-11,Figure2-12, Figure2-13, Figure2-14 and Table 2-3.

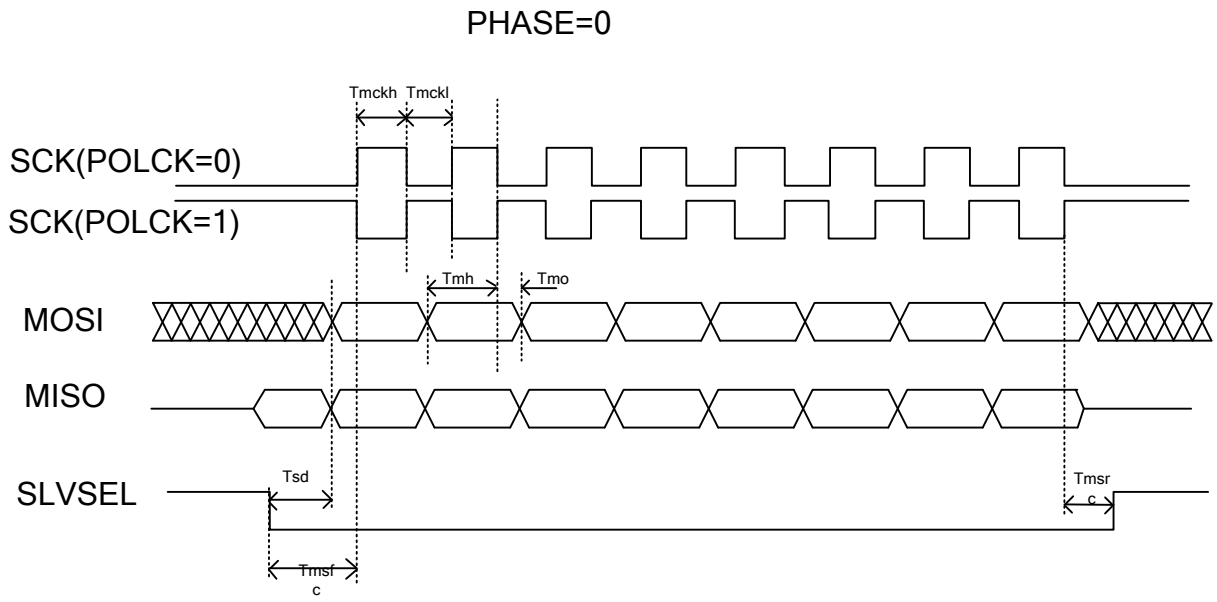


Figure 2-11 SPI master Timing PHASE =0

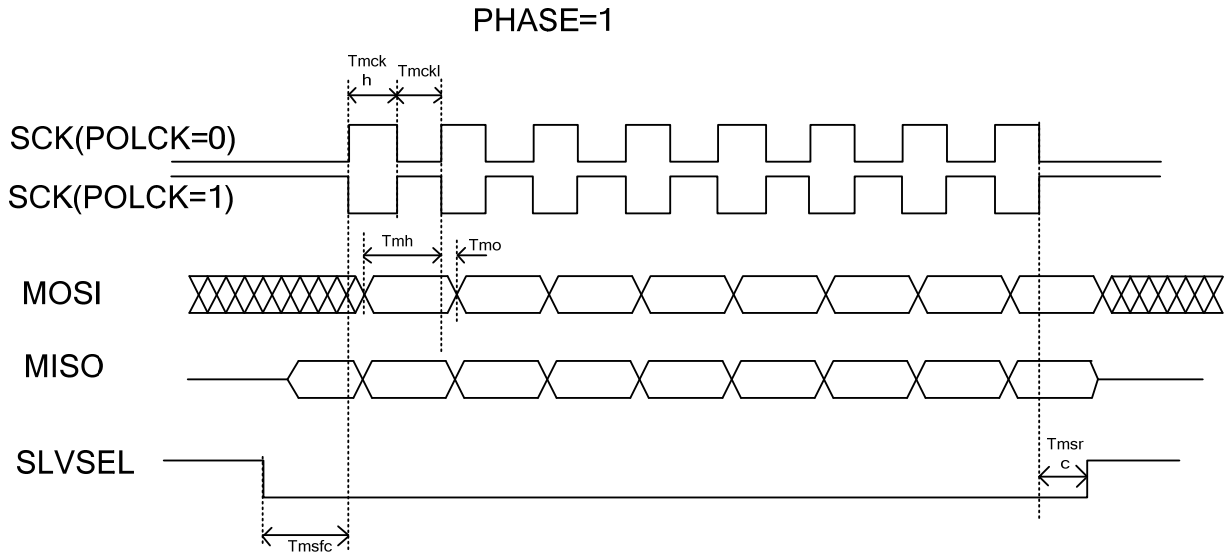


Figure 2-12 SPI master Timing PHASE =1

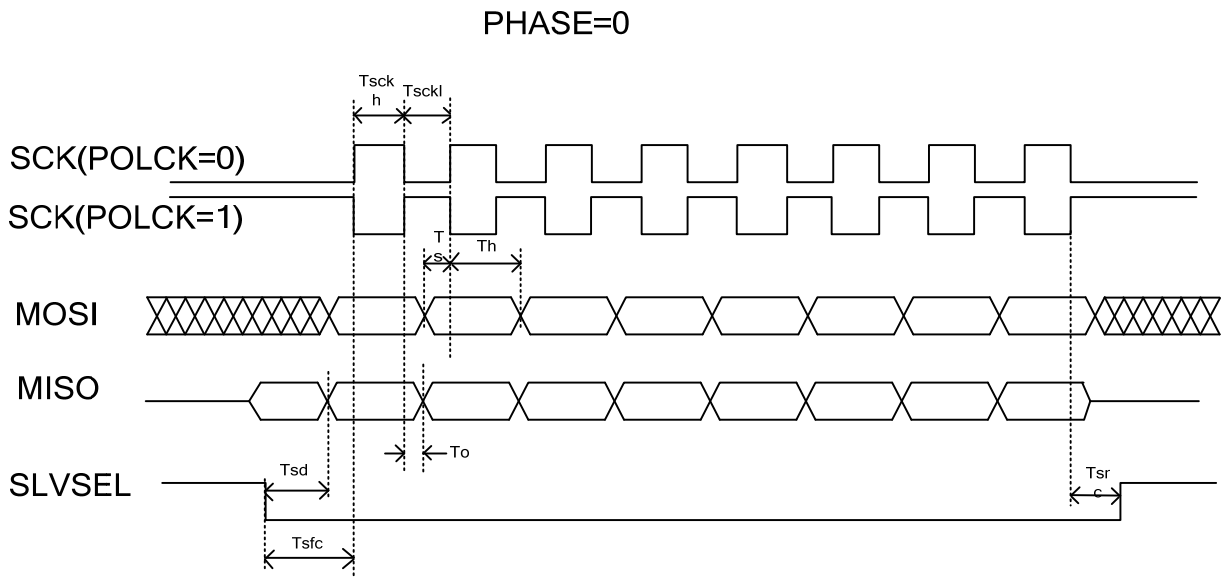


Figure 2-13 SPI slave Timing PHASE = 0

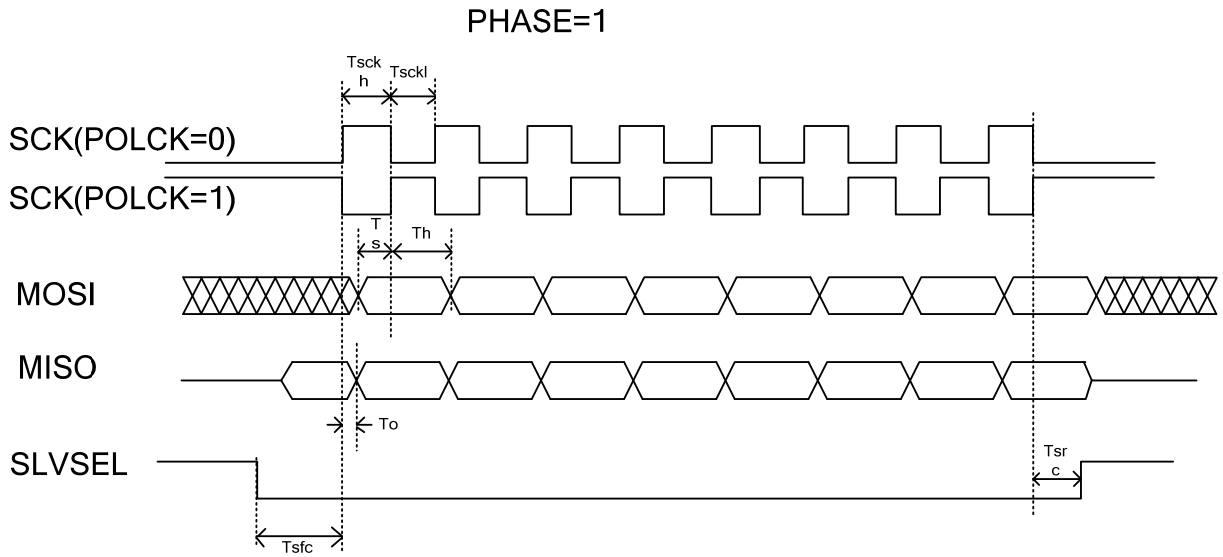


Figure 2-14 SPI slave Timing PHASE = 1

Table 2-3 SPI Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode timing (see figure 2-11,2-12)				
Tmckh	sck high time	4×Tsysclk	--	ns
Tmckl	sck low time	4×Tsysclk	--	ns
Tmo	sck shift edge to mosi data change	0	--	ns
Tmh	mosi data valid to sck shift edge	3×Tsysclk	--	ns
Tsd	slvsel falling edge to mosi data valid	4×Tsysclk	--	ns
Tmsfc	slvsel falling edge to first sck edge	(Tmckh+Tmckl)/	--	ns

		2		
Tmsrc	last sck edge to slvsel rising edge	(Tmckh+Tmckl)/2	--	ns
Slave mode timing(See figure 2-13,2-14)				
Tsckh	sck high Time	4×Tsysclk	--	ns
Tsckl	sck low Time	4×Tsysclk	--	ns
Tsd	slvsel falling edge to Miso valid data time	0	4xTsysclk	ns
Ts	Mosi Data valid to sck sample edge	0	--	ns
Th	sck sample edge to Mosi data change	4×Tsysclk	--	ns
To	sck shift edge to Miso data change	0	4xTsysclk	ns
Tsfc	slvsel falling edge to first sck edge	4×Tsysclk	--	ns
Tsrc	last sck edge to slvsel rising edge	4×Tsysclk	--	ns
*Tsysclk is equal to one period of the device system clock				

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDDA - VSSA	V	-0.3 ~ +3.6	1, 2
Power Supply Voltage 2	VDD3 – VSS	V	-0.3 ~ +3.6	1, 3
I/O Digital Voltage	IOVCC	V	1.8~3.6	1
Operating Temperature	Topr	℃	-20 ~ +85	1
Storage Temperature	Tstg	℃	-55 ~ +150	1

Notes
1.If used beyond the absolute maximum ratings, FT5x16 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2.Make sure VDDA(high)≥VSSA (low)
3.Make sure VDD (high)≥VSS (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics (VDDA=VDD3=2.8~3.6V, Ta=-20~85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=-0.1mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOH=0.1mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	μA	Vin=0~VDDA	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	TBD	--	
Current consumption （Monitor mode）	Imon	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	TBD	--	
Current consumption （Sleep mode）	Islp	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	TBD	--	
Step-up output voltage	VDD5	V	VDDA=VDD3= 2.8V	4.5	5	5.2	1
Power Supply voltage	VDDA VDD3	V		2.8	--	3.6	

Notes

1.If VDDA and VDD3 are 3.3V, the max value of VDD5 is 6V.

3.3 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V Ta=25℃	23.5	24	24.5	

Table 3-4 AC Characteristics of TX & RX

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Note
TX acceptable clock	ftx	KHz		100	150	300	
TX output rise time	Ttxr	nS		--	140	--	
TX output fall time	Ttxf	nS		--	140	--	
RX input voltage	Trxi	V		1.2	--	1.6	

3.4 I/OPortsCircuits

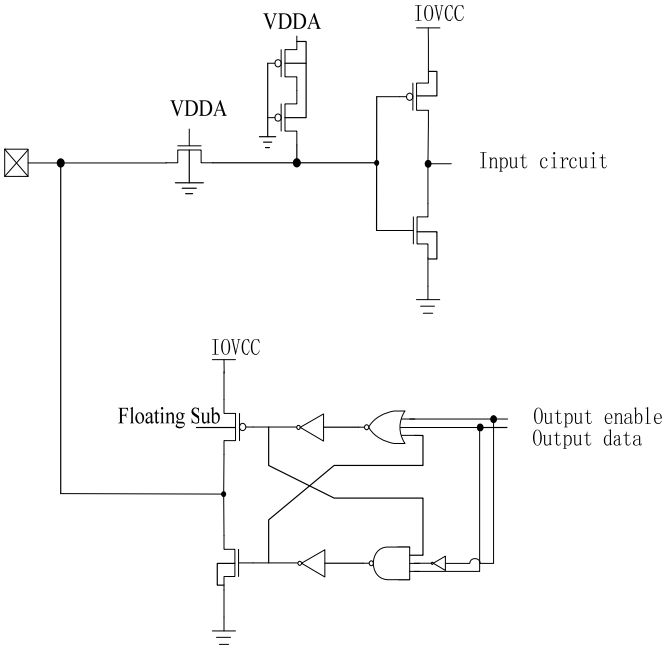


Figure 3-1 Digital In/Out Port Circuit

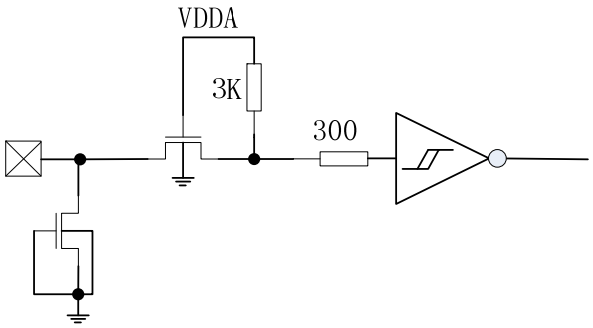


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset/Wake Sequence

Reset should be pulled down to be low before powering on and powering down. INT signal will be sent to the host after initializing all parameters and then start to report points to the host.

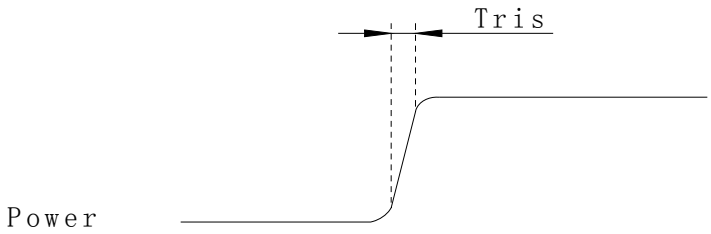


Figure 3-7 Power on time

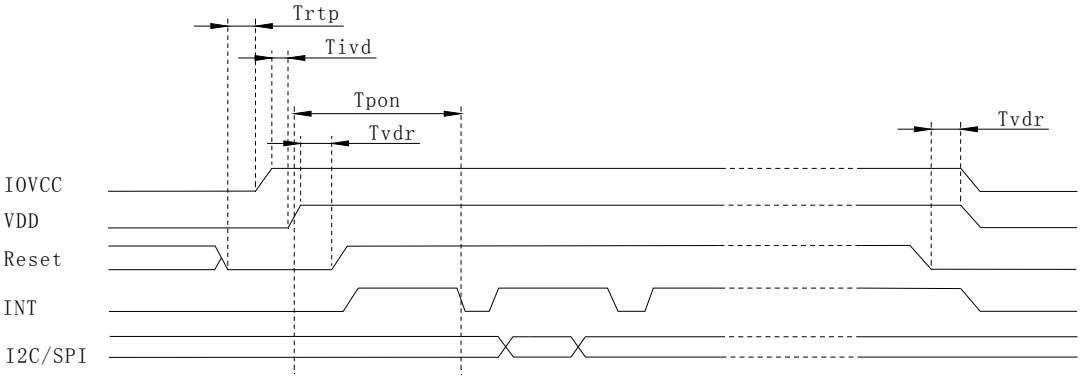


Figure 3-8 Power on Sequence

Reset time must be enough to guarantee reliable reset, The time of starting to report point after resetting approach to the time of starting to report point after powering on.

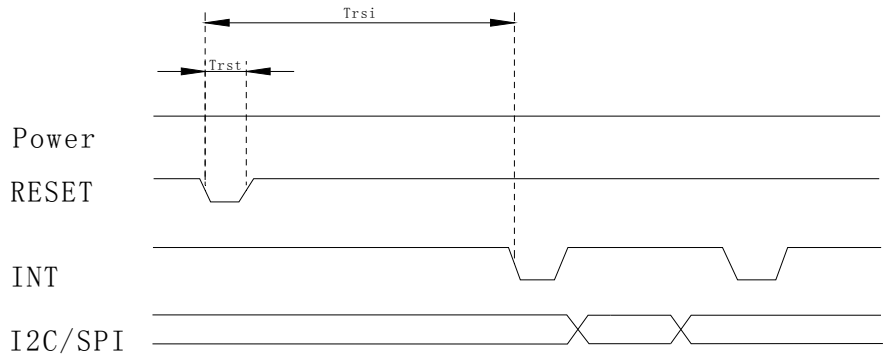


Figure 3-9 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tivd	Delay time of VDD powering on after IOVCC powering on	10	--	μs
Tpon	Time of starting to report point after powering on	200	--	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	1	--	ms

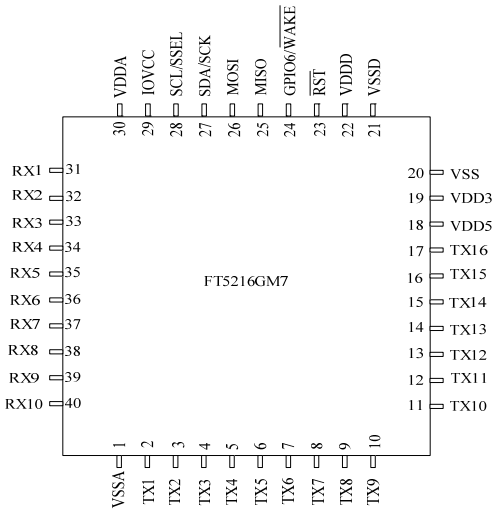
4 PIN CONFIGURATIONS

Pin List of FT5x16

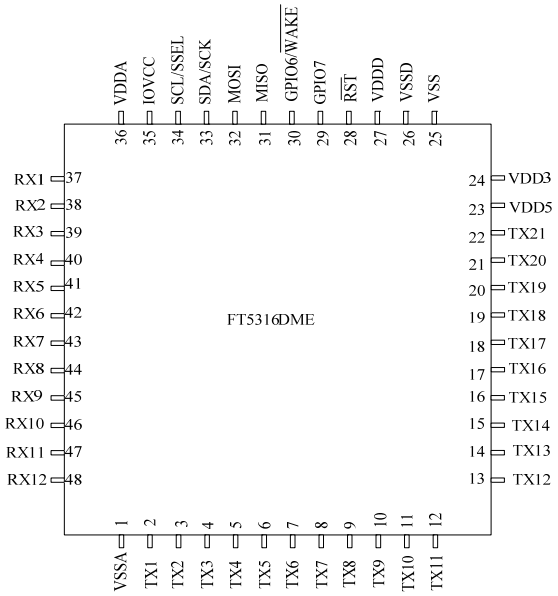
Table 4-1 Pin Definition of FT5x16

Name	Pin No.		Type	Description
	FT5216GM7	FT5316DME		
VSSA	1	1	PWR	Analog ground
TX1	2	2	O	Transmit output pin
TX2	3	3	O	Transmit output pin
TX3	4	4	O	Transmit output pin
TX4	5	5	O	Transmit output pin
TX5	5	6	O	Transmit output pin
TX6	7	7	O	Transmit output pin
TX7	8	8	O	Transmit output pin
TX8	9	9	O	Transmit output pin
TX9	10	10	O	Transmit output pin
TX10	11	11	O	Transmit output pin
TX11	12	12	O	Transmit output pin
TX12	13	13	O	Transmit output pin
TX13	14	14	O	Transmit output pin
TX14	15	15	O	Transmit output pin
TX15	16	16	O	Transmit output pin
TX16	17	17	O	Transmit output pin
TX17		18	O	Transmit output pin
TX18		19	O	Transmit output pin
TX19		20	O	Transmit output pin
TX20		21	O	Transmit output pin
TX22		22	O	Transmit output pin
VDD5	18	23	PWR	internal generated 5V power supply， A 1μF ceramic capacitor to ground is required.
VDD3	19	24	PWR	Analog power supply
VSS	20	25	PWR	Analog ground
VSSD	21	26	PWR	Digital ground
VDDD	22	27	PWR	Digital power supply , generated internal. A 1μF ceramic capacitor to ground is required.
$\overline{\text{RST}}$	23	28	I	External Reset, active low
GPIO7		29	I/O	General Purpose Input/Output port
GPIO6/ $\overline{\text{Wake}}$	24	30	I/O	Interrupt request to the host / Wakeup request from the host
MISO	25	31	I/O	SPI Slave mode, data output
MOSI	26	32	I/O	SPI Slave mode, data input
SDA/SCK	27	33	I/O	I2C data input and output / SPI Slave mode, clock input

SCL/SSEL	28	34	I/O	I2C clock input / SPI Slave mode, chip select, active low
IOVCC	29	35	PWR	I/O power supply
VDDA	30	36	PWR	Analog power supply
RX1	31	37	I	Receiver input pins
RX2	32	38	I	Receiver input pins
RX3	33	39	I	Receiver input pins
RX4	34	40	I	Receiver input pins
RX5	35	41	I	Receiver input pins
RX6	36	42	I	Receiver input pins
RX7	37	43	I	Receiver input pins
RX8	38	44	I	Receiver input pins
RX9	39	45	I	Receiver input pins
RX10	40	46	I	Receiver input pins
RX11		47	I	Receiver input pins
RX12		48	I	Receiver input pins



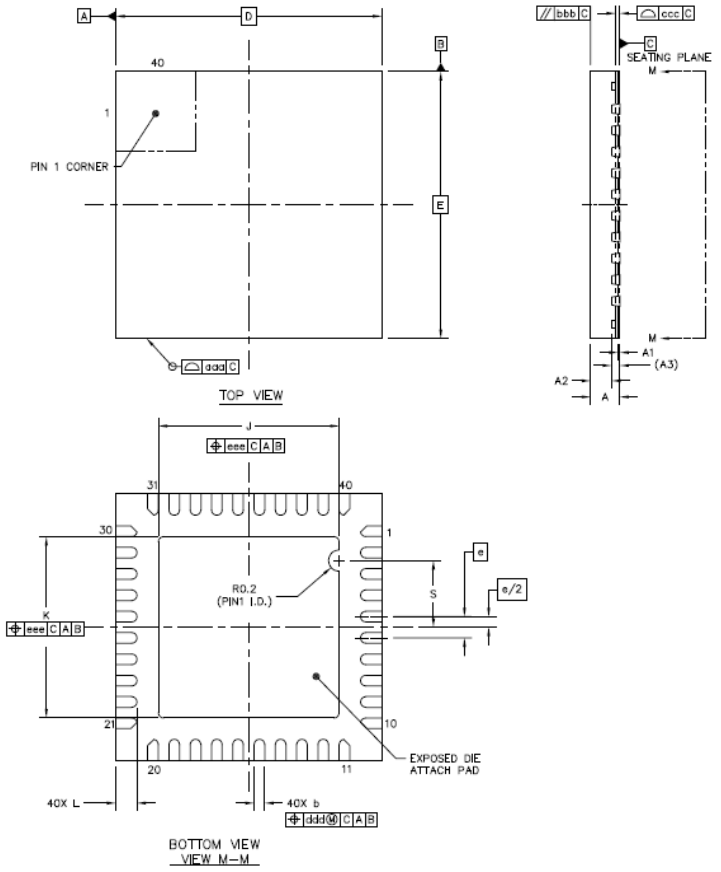
FT5216GM7 Package Diagram



FT5316DME Package Diagram

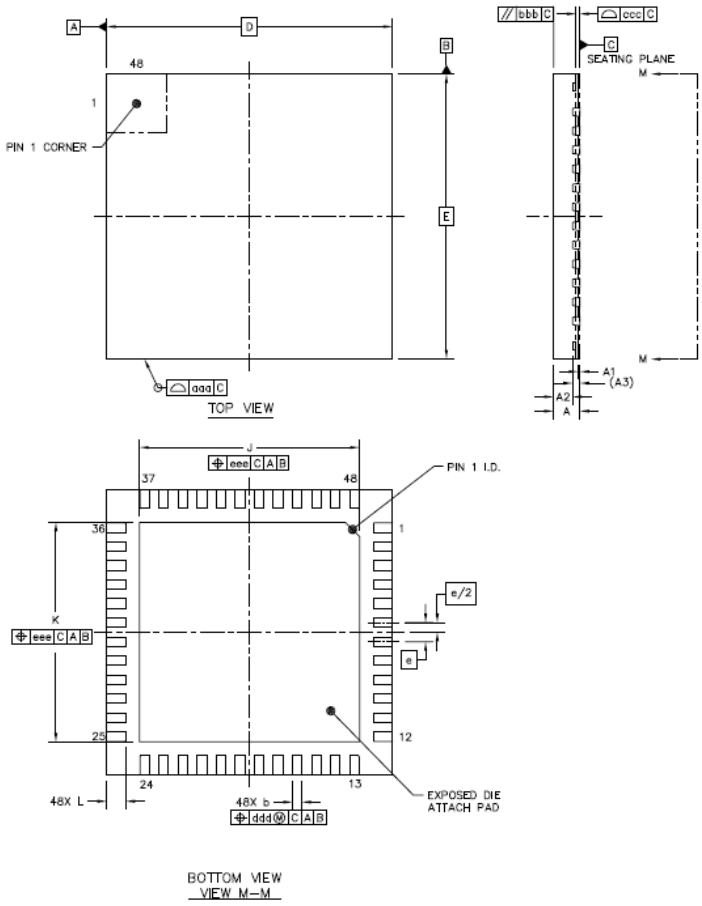
5 PACKAGE INFORMATION

5.1 Package Information of QFN-5x5-40L Package



Item	Symbol	Millimeter		
		Min	Typ	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	0.425
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		5 BSC	
	E		5 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	3.3	3.4	3.5
	K	3.3	3.4	3.5
Lead Length	L	0.35	0.4	0.45
	S	1.15	1.25	1.35
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.2 Package Information of QFN-6x6-48L Package



Item	Symbol	Millimeter		
		Min	Typ	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	0.425
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		6 BSC	
	E		6 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	4.52	4.62	4.72
	K	4.52	4.62	4.72
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.3 Order Information

Package Type	QFN
	40Pin(5 * 5)/48Pin(6 * 6)
	0.55 - P0.4
Product Name	FT5216GM7/ FT5316DME

Note:

1). The last three letters in the product name indicate the package type and lead pitch and thickness.

2). The three last letter indicates the package type.
D : QFN-6*6 , **G** : QFN-5*5

3). The second last letter indicates the lead pitch and thickness.
M : 0.55 - P0.4

4). The last letter indicates the numbers of TX and RX.
7: 16TX-10RX , **E**: 21TX-12RX

T: Track Code

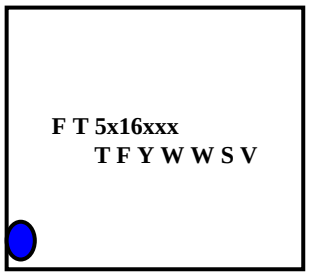
F/R: ”F” for Lead Free process,
”R” for Halogen Free process

Y: Year Code

WW: Week Code

S: Lot Code

V：IC Version



Product Name	Package Type	# TX Pins	# RX Pins
FT5216GM7	QFN-40L	16	10
FT5316DME	QFN-48L	21	12

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