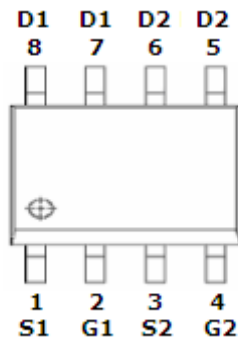


**DESCRIPTION**

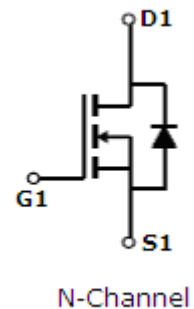
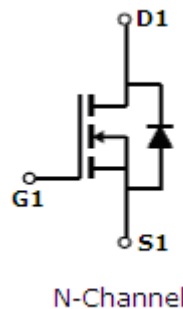
The ST4828N is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application , notebook computer Li-ion Battery , power management and other battery powered circuits where high-side switching .

**PIN CONFIGURATION**  
**SOP-8**

**FEATURE**

- 60V/10A,  $R_{DS(ON)} = 30m\Omega$  (Typ.) @VGS = 10V
- 60V/6A,  $R_{DS(ON)} = 35m\Omega$  @VGS = 4.5V
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

**PART MARKING**  
**SOP-8**


Y: Year Code A: Process Code





**ST4828N** 

Dual N Channel Enhancement Mode MOSFET  
**10A**

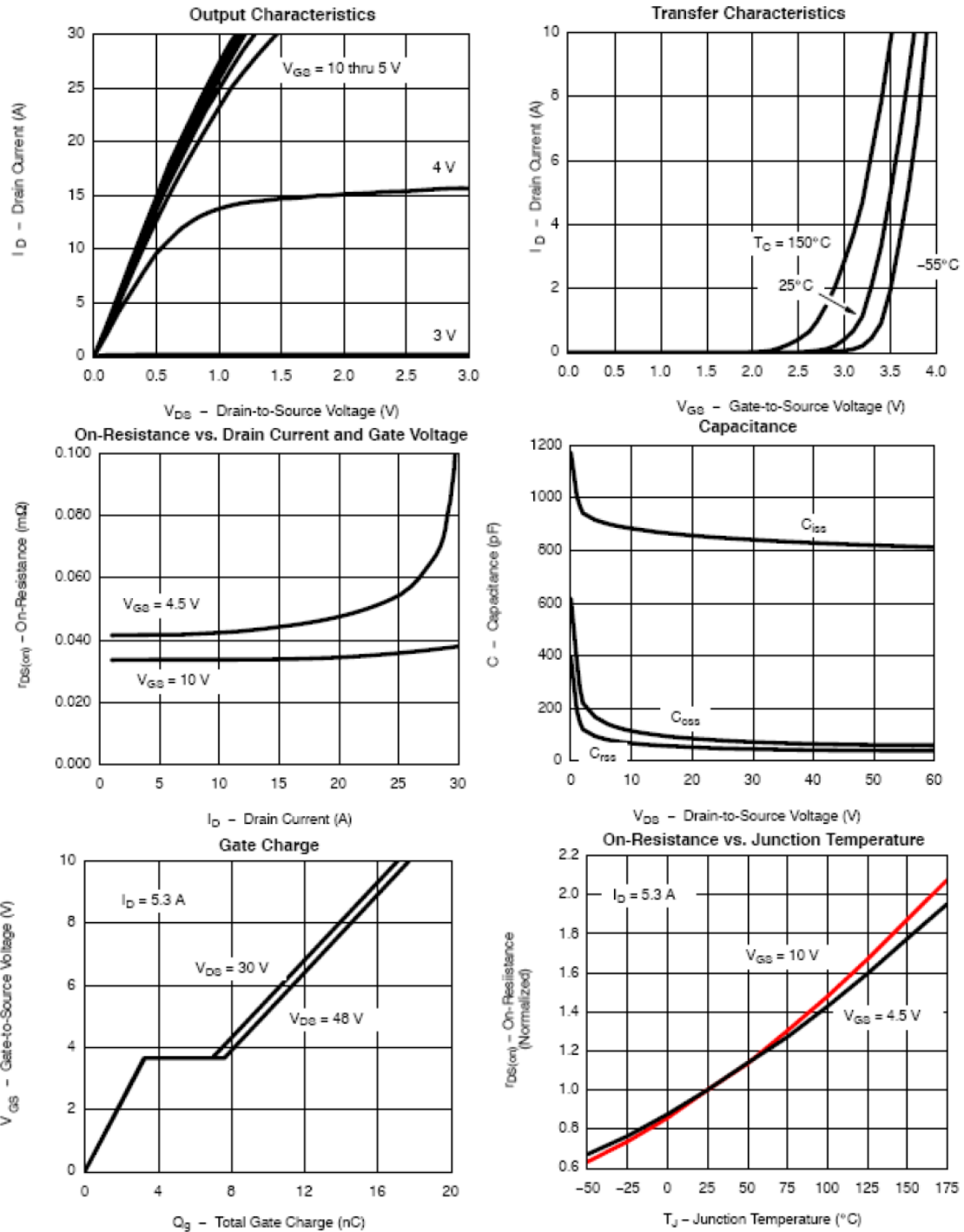
**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C 8.0	A
		T <sub>A</sub> =70°C 6.0	
Pulsed Drain Current	I <sub>DM</sub>	30	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	11	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 2.5	W
		T <sub>A</sub> =70°C 1.6	
Operation Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	80	°C/W

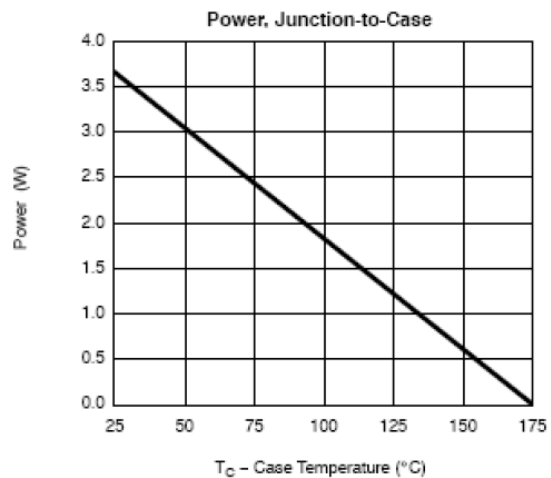
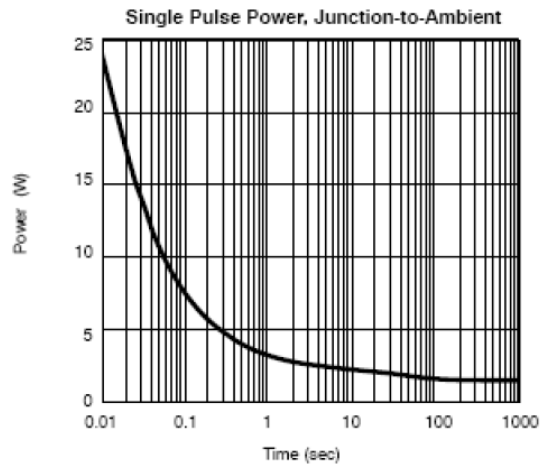
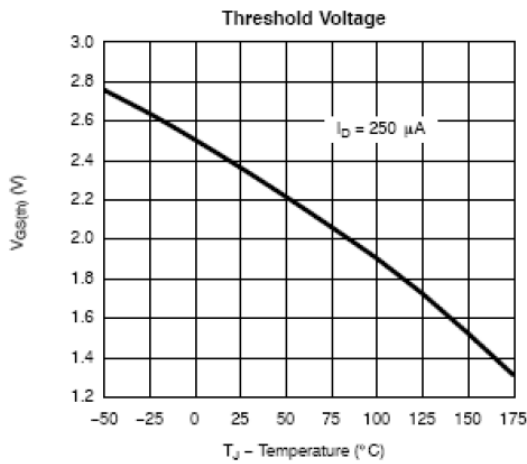
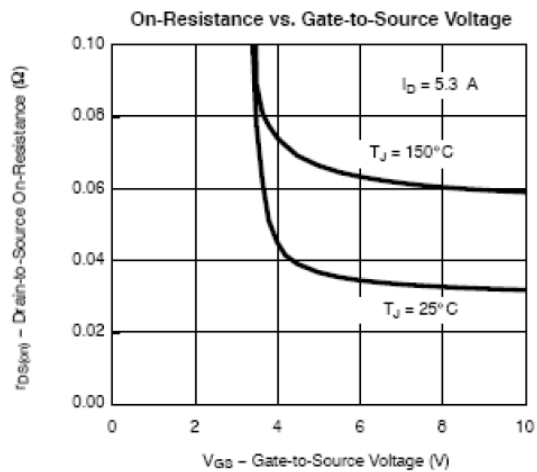
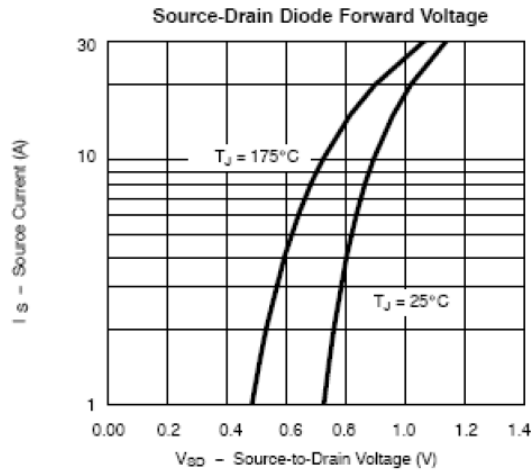


**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

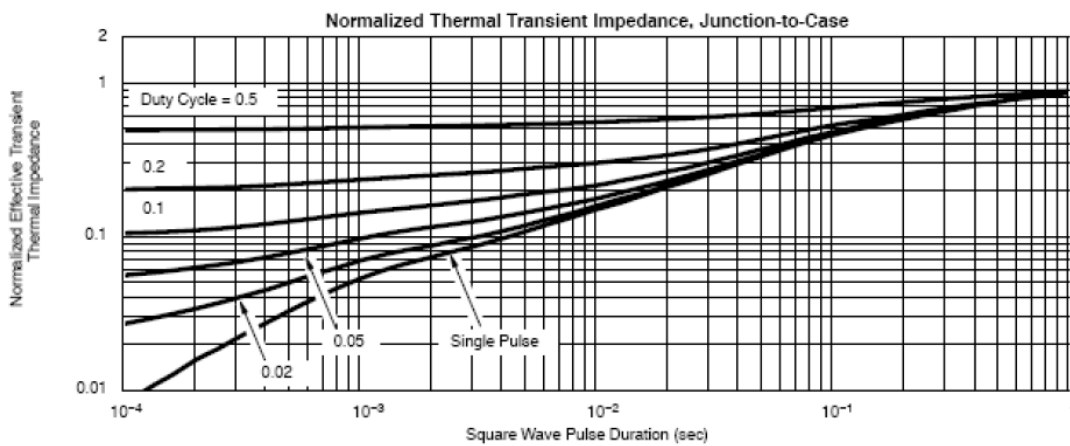
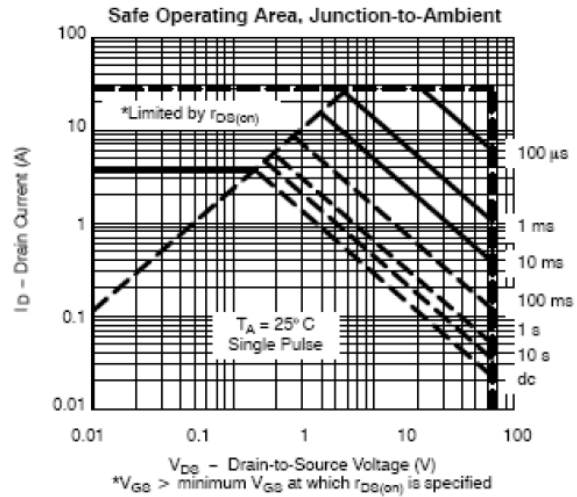
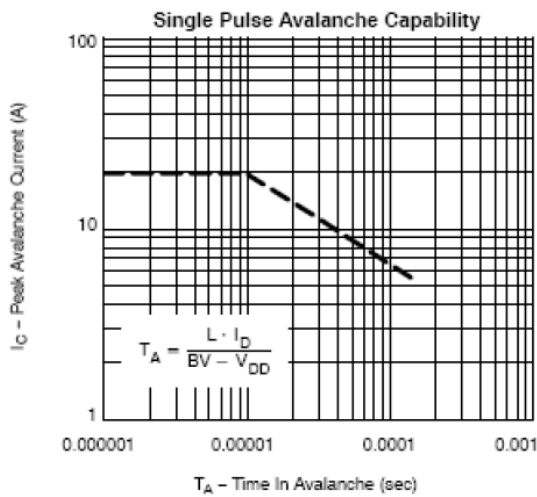
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250 \mu A$	0.1		3.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$ $T_J=55^\circ C$	$V_{DS}=60V, V_{GS}=0V$			1	uA
		$V_{DS}=60V, V_{GS}=0V$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq 5V, V_{GS}=10V$	25			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$		0.030		$\Omega$
		$V_{GS}=4.5V, I_D=6A$		0.035		
Forward Tran Conductance	$g_{fs}$	$V_{DS}=5.0V, I_D=5.3A$		24		S
Diode Forward Voltage	$V_{SD}$	$I_S=1.7A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}= 5V$ $I_D=5.3A$		10		nC
Gate-Source Charge	$Q_{gs}$			3.5		
Gate-Drain Charge	$Q_{gd}$			3.6		
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V$ $f=1MHz$		890		pF
Output Capacitance	$C_{oss}$			84		
Reverse TransferCapacitance	$C_{rss}$			49		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DD}=30V, R_L=6.8\Omega$ $I_D=4.4A, V_{GEN}=10V$ $R_G=1\Omega$		10	14	nS
				15	20	
Turn-Off Time	$t_{d(off)}$ $t_f$			25	35	
				10	15	

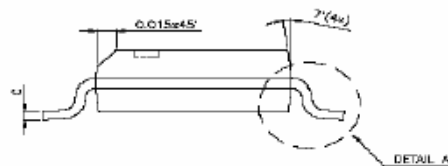
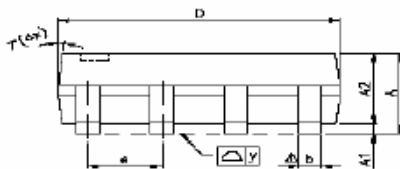
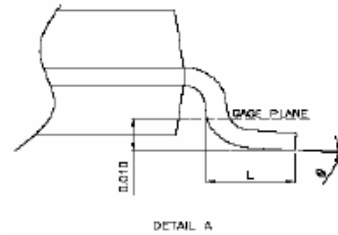
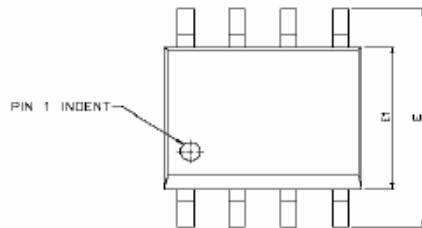
**TYPICAL CHARACTERISTICS (25°C Unless Note)**


**TYPICAL CHARACTERISTICS** (25°C Unless Note)



**TYPICAL CHARACTERISTICS** (25°C Unless Note)



**SOP-8 PACKAGE OUTLINE**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
$\Delta$ y	—	—	0.076	—	—	0.003
$\phi$	0°	—	8°	0°	—	8°