EPSON

SRM2B256SLMT55/70/10

256K-Bit Static RAM

Wide Voltage Operation Products

- Wide Temperature Range
- Extremely Low Standby Current
- Access Time 100ns (2.7V) /55ns (4.5V)
- 32,768 Words x 8-bit Asynchronous

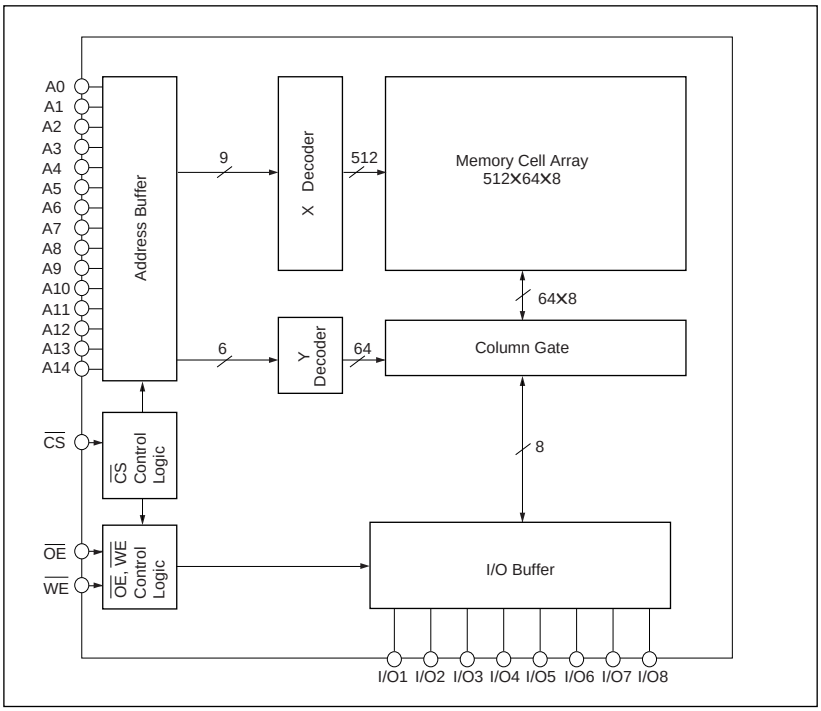
■ DESCRIPTION

The SRM2B256SLMT is a low voltage operating 32,768 words×8-bit asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power consumption makes it ideal for applications requiring non-volatile storage with back-up batteries. And –40 to 85°C operating temperature range makes it ideal for industrial use. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Output ports are 3-state output allows easy expansion of memory capacity. These features makes the SRM2B256SLMT usable for wide range of applications from microprocesser systems to terminal devices.

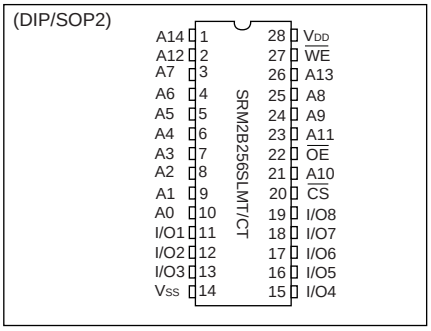
■ FEATURES

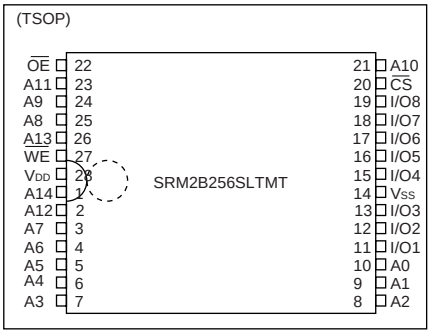
- Wide temperature range ..... –40 to 85°C
- Extended supply voltage range ..... 2.7 to 5.5V
- Fast access time ..... 100ns (3V±10%)
  55ns (5V±10%)
- Extremely low standby current ..... SL Version
- Completely static ..... no clock required
- 3-state output
- Battery back-up operation
- Package ..... SRM2B256SLCT DIP2-28pin (plastic)
  SRM2B256SLMT SOP2-28pin (plastic)
  SRM2B256SLTMT TSOP (I) -28pin (plastic)
  SRM2B256SLRMT TSOP (I) -28pin-R1 (plastic)

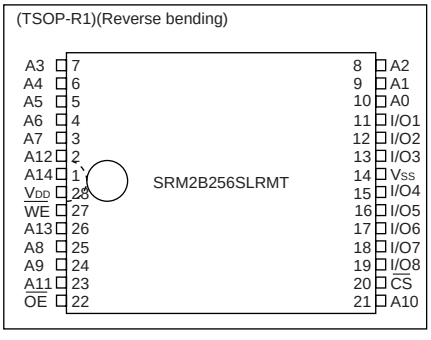
■ BLOCK DIAGRAM



■ PIN CONFIGURATION







■ PIN DESCRIPTION

A0 to A14	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to I/O8	Data Input/Output
V_{DD}	Power Supply (2.7 to 5.5V)
V_{SS}	Power Supply (0V)

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■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage	V_I	–0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	–0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	–40 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s(Lead only)	–

*V_I, $V_{I/O}$ (Min.)= – 3.0V when pulse width is less or equal to 50ns

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta= –40 to 85°C)

Parameter	Symbol	V_{DD}=3V±10%			V_{DD}=5V±10%			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V_{DD}	2.7	–	3.3	4.5	–	5.5	V
	V_{SS}	0	–	0	0	–	0	V
Input voltage	V_{IH}	2.2	–	V_{DD}+0.3	2.2	–	V_{DD}+0.3	V
	V_{IL}	–0.3*	–	0.4	–0.3*	–	0.8	V

*V_{IL} (Min.)= –3V when pulse width is less or equal to 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{SS}=0V, Ta= –40 to 85°C)

Parameter	Symbol	Conditions	V_{DD}=3V±10%			V_{DD}=5V±10%			Unit
			Min.	Typ.*1	Max.	Min.	Typ.*2	Max.	
Input leakage	I_{LI}	V_I=0 to V_{DD}	–1.0	–	1.0	–1.0	–	1.0	µA
Standby supply current	I_{DDS}	$\overline{CS}$=V_{IH}	–	–	2	–	–	3	mA
	I_{DDS1}	$\overline{CS}$≥V_{DD}–0.2V	–	0.3	25	–	0.5	50	µA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA, t_{cyc}=Min.	–	10	15	–	30	45	mA
	I_{DDA1}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA, t_{cyc}=1µs	–	–	5	–	–	10	mA
Operating supply current	I_{DDO}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA	–	–	5	–	–	10	mA
Output leakage	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	–1.0	–	1.0	–1.0	–	1.0	µA
High level output voltage	V_{OH}	I_{OH}=–1.0mA, –0.5mA*3	2.4	–	–	2.4	–	–	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA, 1.0mA*3	–	–	0.4	–	–	0.4	V

*1 Typical values are measured at Ta=25°C and V_{DD}=3.0V
*2 Typical values are measured at Ta=25°C and V_{DD}=5.0V
*3 V_{DD}=3V±10%

● Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_I	V_I=0V	–	–	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	10	pF

Note : This parameter is made by the inspection data of sample, not for all products.

● AC Electrical Characteristics

❍ Read Cycle

(V_{SS}=0V, Ta=–40 to 85°C)

Parameter	Symbol	Conditions	SRM2B256SLMT55				SRM2B256SLMT70				SRM2B256SLMT10				Unit
			V_{DD}=3V±10%		V_{DD}=5V±10%		V_{DD}=3V±10%		V_{DD}=5V±10%		V_{DD}=3V±10%		V_{DD}=5V±10%		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	*1	100	–	55	–	120	–	70	–	180	–	100	–	nS
Address access time	t_{ACC}		–	100	–	55	–	120	–	70	–	180	–	100	nS
$\overline{CS}$ access time	t_{ACS}		–	100	–	55	–	120	–	70	–	180	–	100	nS
$\overline{OE}$ access time	t_{OE}		–	60	–	30	–	70	–	35	–	90	–	45	nS
$\overline{CS}$ output set time	t_{CLZ}	*2	15	–	10	–	15	–	10	–	15	–	10	–	nS
$\overline{CS}$ output floating	t_{CHZ}		–	35	–	20	–	40	–	25	–	50	–	35	nS
$\overline{OE}$ output set time	t_{OLZ}		5	–	5(0)	–	5	–	5(0)	–	5	–	5(0)	–	nS
$\overline{OE}$ output floating	t_{OHZ}		–	35	–	20	–	40	–	25	–	50	–	35	nS
Output hold time	t_{OH}	*1	15	–	10	–	15	–	10	–	15	–	10	–	nS

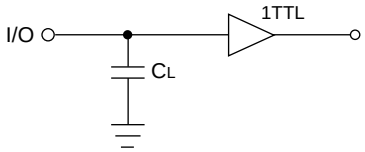
❍ Write Cycle

(V_{SS}=0V, Ta=–40 to 85°C)

Parameter	Symbol	Conditions	SRM2B256SLMT55				SRM2B256SLMT70				SRM2B256SLMT10				Unit
			V_{DD}=3V±10%		V_{DD}=5V±10%		V_{DD}=3V±10%		V_{DD}=5V±10%		V_{DD}=3V±10%		V_{DD}=5V±10%		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	*1	100	–	55	–	120	–	70	–	180	–	100	–	nS
Chip select time	t_{CW}		80	–	50	–	90	–	60	–	110	–	80	–	nS
Address valid to end of write	t_{AW}		80	–	50	–	90	–	60	–	110	–	80	–	nS
Address setup time	t_{AS}		0	–	0	–	0	–	0	–	0	–	0	–	nS
Write pulse width	t_{WP}		75	–	40	–	80	–	45	–	100	–	60	–	nS
Address hold time	t_{WR}		0	–	0	–	0	–	0	–	0	–	0	–	nS
Input data set time	t_{DW}		40	–	25	–	45	–	30	–	60	–	40	–	nS
Input data hold time	t_{DH}		0	–	0	–	0	–	0	–	0	–	0	–	nS
Write to Output floating	t_{WHZ}	*2	–	35	–	20	–	40	–	25	–	50	–	35	nS
Output Active from end to wirte	t_{OW}		5	–	5	–	5	–	5	–	5	–	5	–	nS

*1 Test Conditions

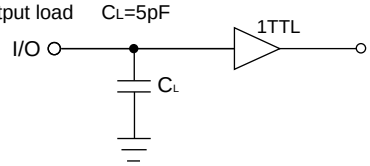
1. Input pulse level: 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L=100pF



C_L=100pF (Includes Jig Capacitance)

*2 Test Conditions

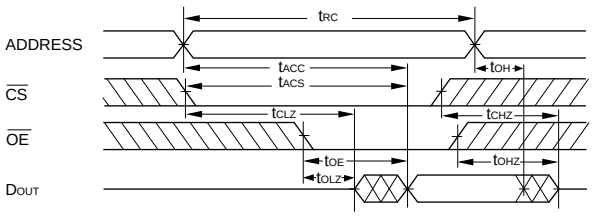
1. Input pulse level : 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels:
   ±200mV (the level displaced from stable output voltage level)
5. Output load C_L=5pF



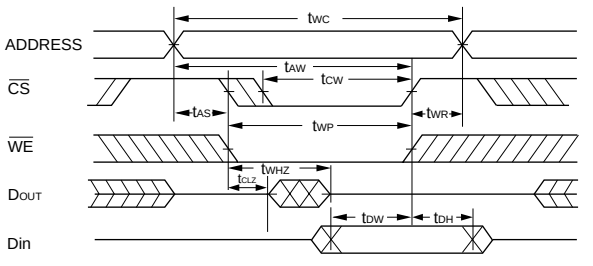
C_L=5pF (Includes Jig Capacitance)

● Timing chart

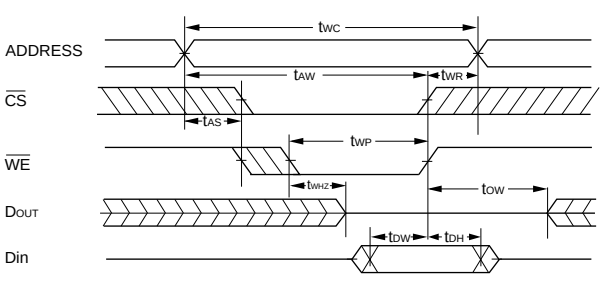
❍ Read Cycle*1



❍ Write Cycle (1)($\overline{CS}$ Control)*2



❍ Write Cycle (2)($\overline{WE}$ Control)*3, *4



Note :

* 1 During read cycle time, $\overline{WE}$ is to be "H" level.
* 2 During write cycle time that is controlled by $\overline{CS}$, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".
* 3 During write cycle time that is controlled by $\overline{WE}$, Output Buffer is in high impedance state if $\overline{OE}$ is "H" level.
* 4 When I/O terminals are output mode, be careful that do not give the opposite signals to the terminals.

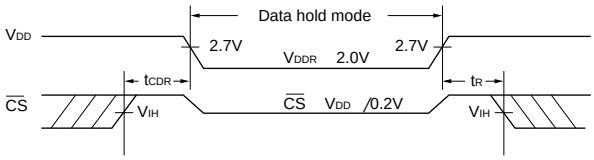
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V_{SS}=0V, Ta=–40 to 40°C)

Parameter	Symbol	Conditions		Min.	Typ.*1	Max.	Unit
Data retention Supply voltage	V_{DDR}			2.0	–	5.5	V
Data retention current	I_{DDR}	V_{DD}=3V, $\overline{CS}\geq V_{DD}-0.2V$	–40 to 85°C	–	0.25	20	µA
			0 to 70°C	–	0.25	10	µA
			0 to 40°C	–	0.25	2	µA
Chip select data hold time	t_{CDR}			0	–	–	ns
Operation recovery time	t_R			5	–	–	ms

*1 Typical values are measured at 25 °C

Data retention timing



Note: During standby mode in which the data is retentive, the supply voltage (V_{DD}) can be in low voltage until V_{DD}=V_{DDR}.
At this mode data reading and writing are impossible.

■ FUNCTIONS

● Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	Mode	I_{DD}
H	X	X	—	Hi-Z	Standby	I_{DDS}, I_{DDS1}
L	X	L	Stable	D_{IN}	Write	I_{DDA}, I_{DDA1}
L	L	H	Stable	D_{OUT}	Read	I_{DDA}, I_{DDA1}
L	H	H	Stable	Hi-Z	Output disable	I_{DDA}, I_{DDA1}

X : "H" or "L", – "H", "L" or "Hi-Z"

● Read Mode

The data appear when the address is set while holding $\overline{CS}$="L" $\overline{OE}$="L" and $\overline{WE}$="H". When $\overline{OE}$="H", DATA I/O terminals are in high impedance state, that makes circuit design and bus control easy.

● Write Mode

There are the following 3 ways of writing data into memory.

(1) Hold $\overline{CS}$="L" and $\overline{WE}$="L", set address

(2) Hold $\overline{CS}$="L" then set address and give "L"pulse to $\overline{WE}$.

(3) After setting addresses, give "L"pulse to both $\overline{CS}$ and $\overline{WE}$.

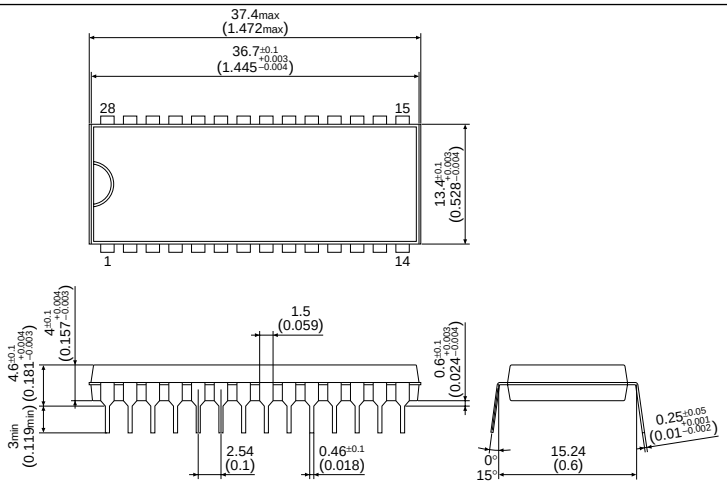
In above any case data on the DATA I/O terminals are latched up into the chip when $\overline{CS}$ or $\overline{WE}$ is in positive-going. Since DATA I/O terminals are high impedance when $\overline{CS}$ or $\overline{OE}$="H", bus contention between data driver and memory outputs can be avoided.

● Standby Mode

When $\overline{CS}$ is "H" the chip become in the standby mode. In this mode, DATA I/O terminals are high impedance and all inputs of addresses, $\overline{WE}$ and data can be any "H"or "L". When $\overline{CS}$ is over than V_{DD}-0.2V, the chip is in the data retention battery backup mode, in this case, there is a small current in the chip which flow through the high resistances of the memory cells.

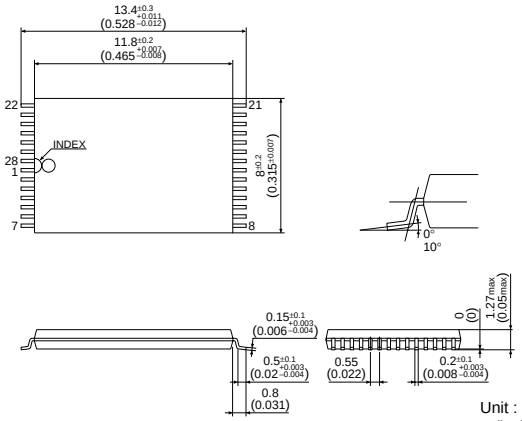
■ PACKAGE DIMENSIONS

Plastic DIP-28pin



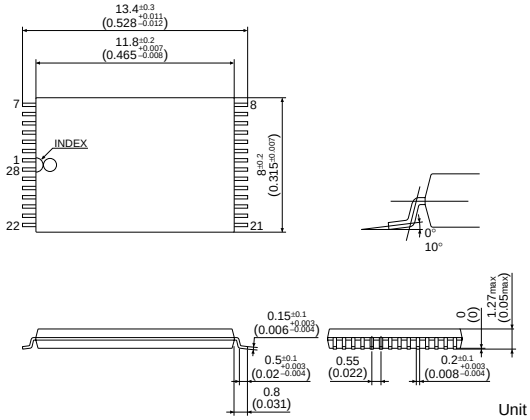
Unit : mm
(inch)

Plastic TSOP(I)-28pin



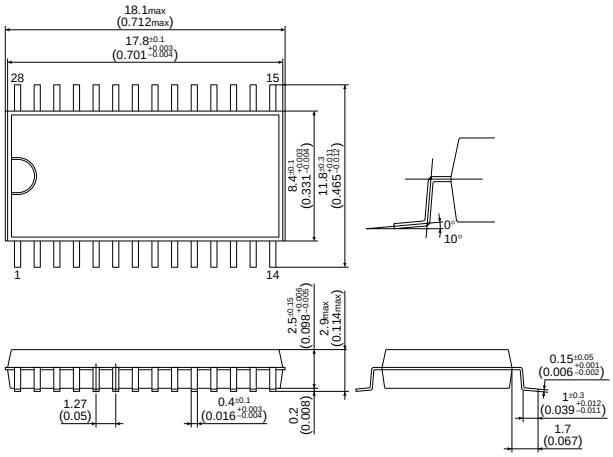
Unit : mm
(inch)

Plastic TSOP(I)-28pin-R1



Unit : mm
(inch)

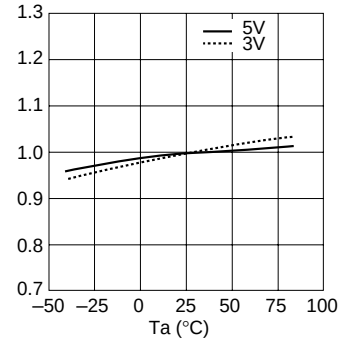
Plastic SOP2-28pin



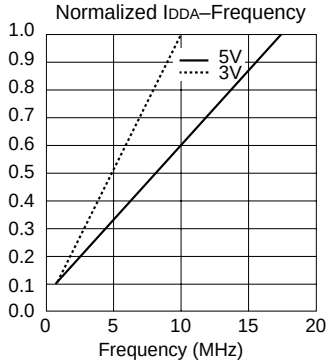
Unit : mm
(inch)

■ CHARACTERISTICS CURVES

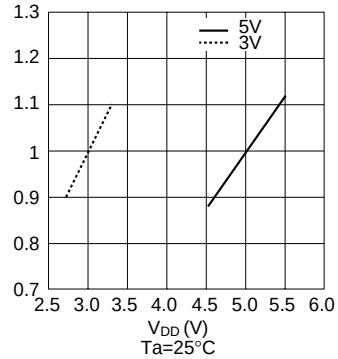
Normalized I_{DDA}–Ta



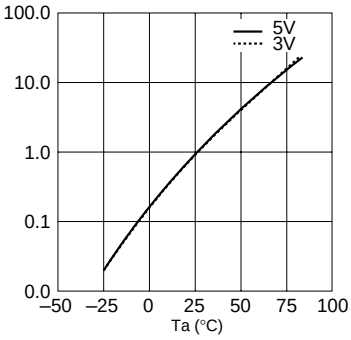
Normalized I_{DDA}–Frequency



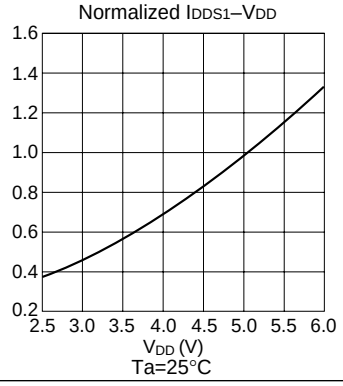
Normalized I_{DDA}–V_{DD}



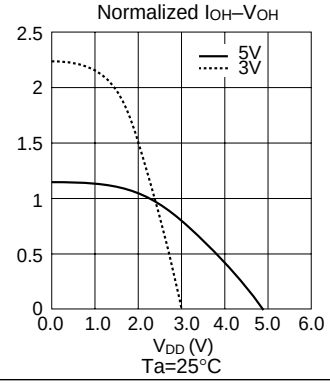
Normalized I_{DDS1}–Ta



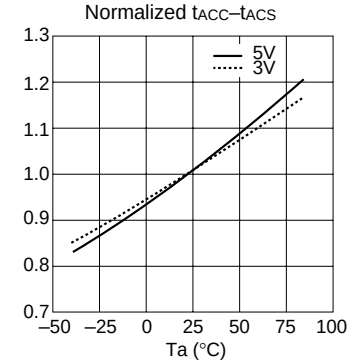
Normalized I_{DDS1}–V_{DD}



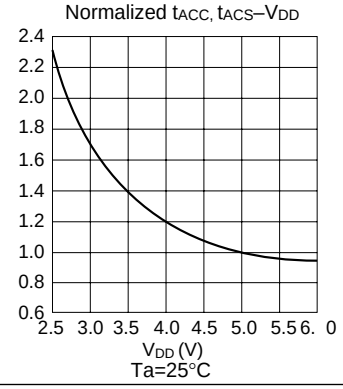
Normalized I_{OH}–V_{OH}



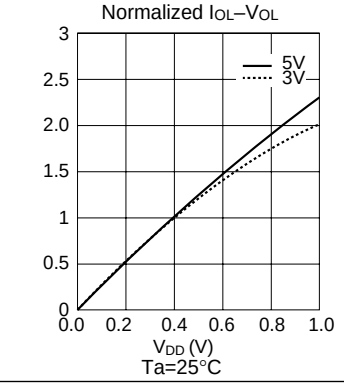
Normalized t_{ACC}–t_{ACS}



Normalized t_{ACC}, t_{ACS}–V_{DD}



Normalized I_{OL}–V_{OL}



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